

# SN74ACT564 Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs

## 1 Features

- Operation of 4.5V to 5.5V  $V_{CC}$
- Inputs accept voltages to 5.5V
- Max  $t_{pd}$  of 8.5ns at 5V
- Inputs are TTL-voltage compatible
- 3-state inverted outputs drive bus lines directly
- Flow-through architecture to optimize PCB layout
- Full parallel access for loading

## 2 Description

The 'ACT564 devices are octal D-type edge-triggered flip-flops that feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

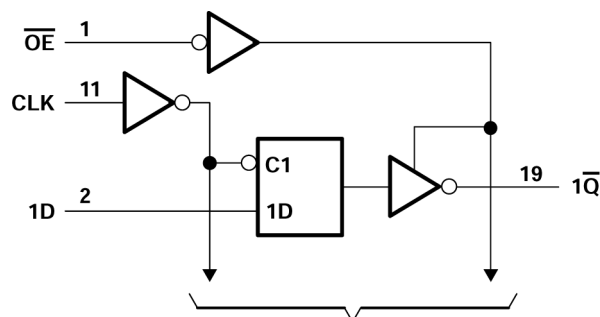
### Package Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE <sup>(2)</sup> | BODY SIZE <sup>(3)</sup> |
|-------------|------------------------|-----------------------------|--------------------------|
| SN74ACT564  | DW (SOIC, 20)          | 12.8mm × 10.3mm             | 12.8mm × 7.5mm           |
|             | N (PDIP, 20)           | 24.33mm × 9.4mm             | 24.33mm × 6.35mm         |
|             | NS (SOP, 20)           | 12.6mm × 7.8mm              | 12.6mm × 5.3mm           |
|             | PW (TSSOP, 20)         | 6.5mm × 6.4mm               | 6.5mm × 4.4mm            |

(1) For more information, see [Section 10](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



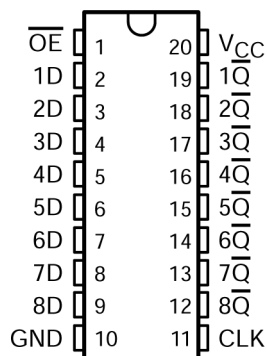
To Seven Other Channels  
Logic Diagram (Positive Logic)



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## 3 Pin Configuration and Functions



**Figure 3-1. SN74ACT564 DB, DW, N, NS, or PW Package (Top View)**

**Table 3-1. Pin Functions**

| PIN |                 | TYPE | Description                    |
|-----|-----------------|------|--------------------------------|
| NO. | NAME            |      |                                |
| 1   | $\overline{OE}$ | I    | Clear all channels, active low |
| 2   | 1D              | I    | Channel 1, D input             |
| 3   | 2D              | I    | Channel 2, D input             |
| 4   | 3D              | I    | Channel 3, D input             |
| 5   | 4D              | I    | Channel 4, D input             |
| 6   | 5D              | I    | Channel 5, D input             |
| 7   | 6D              | I    | Channel 6, D input             |
| 8   | 7D              | I    | Channel 7, D input             |
| 9   | 8D              | I    | Channel 8, D input             |
| 10  | GND             | —    | Ground                         |
| 11  | CLK             | I    | Clock Pin                      |
| 12  | 8Q              | O    | Channel 8, Q output            |
| 13  | 7Q              | O    | Channel 7, Q output            |
| 14  | 6Q              | O    | Channel 6, Q output            |
| 15  | 5Q              | O    | Channel 5, Q output            |
| 16  | 4Q              | O    | Channel 4, Q output            |
| 17  | 3Q              | O    | Channel 3, Q output            |
| 18  | 2Q              | O    | Channel 2, Q output            |
| 19  | 1Q              | O    | Channel 1, Q output            |
| 20  | $V_{CC}$        | —    | Power Pin                      |

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                      |                                            | MIN                                  | MAX            | UNIT    |
|----------------------|--------------------------------------------|--------------------------------------|----------------|---------|
| $V_{CC}$             | Supply voltage range                       | −0.5                                 | 7              | V       |
| $V_I$ <sup>(2)</sup> | Input voltage range                        | −0.5                                 | $V_{CC} + 0.5$ | V       |
| $V_O$ <sup>(2)</sup> | Output voltage range                       | −0.5                                 | $V_{CC} + 0.5$ | V       |
| $I_{IK}$             | Input clamp current                        | $(V_I < 0 \text{ or } V_I > V_{CC})$ |                | ±20 mA  |
| $I_{OK}$             | Output clamp current                       | $(V_O < 0 \text{ or } V_O > V_{CC})$ |                | ±20 mA  |
| $I_O$                | Continuous output current                  | $(V_O = 0 \text{ to } V_{CC})$       |                | ±50 mA  |
|                      | Continuous current through $V_{CC}$ or GND |                                      |                | ±200 mA |
| $T_{stg}$            | Storage temperature range                  | −65                                  | 150            | °C      |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 Recommended Operating Conditions

(over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                     |                                    | SN74ACT564 |          | UNIT |
|---------------------|------------------------------------|------------|----------|------|
|                     |                                    | MIN        | MAX      |      |
| $V_{CC}$            | Supply voltage                     | 4.5        | 5.5      | V    |
| $V_{IH}$            | High-level input voltage           | 2          |          | V    |
| $V_{IL}$            | Low-level input voltage            |            | 0.8      | V    |
| $V_I$               | Input voltage                      | 0          | $V_{CC}$ | V    |
| $V_O$               | Output voltage                     | 0          | $V_{CC}$ | V    |
| $I_{OH}$            | High-level output current          |            | −24      | mA   |
| $I_{OL}$            | Low-level output current           |            | 24       | mA   |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |            | 8        | ns/V |
| $T_A$               | Operating free-air temperature     | −40        | 85       | °C   |

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND for proper device operation. Refer to the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 4.3 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                        | SN74ACT564 |           |          |         |            | UNIT |
|-------------------------------|----------------------------------------|------------|-----------|----------|---------|------------|------|
|                               |                                        | DB (SSOP)  | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) |      |
|                               |                                        | 20 PINS    | 20 PINS   | 20 PINS  | 20 PINS | 20 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance | 70         | 101.2     | 69       | 106.2   | 126.2      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                       | TEST CONDITIONS                                             | V <sub>CC</sub> | T <sub>A</sub> = 25°C |      |       | SN74ACT564 |      | UNIT |
|---------------------------------|-------------------------------------------------------------|-----------------|-----------------------|------|-------|------------|------|------|
|                                 |                                                             |                 | MIN                   | TYP  | MAX   | MIN        | MAX  |      |
| V <sub>OH</sub>                 | I <sub>OH</sub> = –50 µA                                    | 4.5 V           | 4.4                   | 4.49 |       | 4.4        |      | V    |
|                                 |                                                             | 5.5 V           | 5.4                   | 5.49 |       | 5.4        |      |      |
|                                 | I <sub>OH</sub> = –24 mA                                    | 4.5 V           | 3.86                  |      |       | 3.76       |      |      |
|                                 |                                                             | 5.5 V           | 4.86                  |      |       | 4.76       |      |      |
|                                 | I <sub>OH</sub> = –50 mA <sup>(1)</sup>                     | 5.5 V           |                       |      |       |            |      |      |
|                                 | I <sub>OH</sub> = –75 mA <sup>(1)</sup>                     | 5.5 V           |                       |      |       | 3.85       |      |      |
| V <sub>OL</sub>                 | I <sub>OL</sub> = 50 µA                                     | 4.5 V           |                       |      | 0.1   |            | 0.1  | V    |
|                                 |                                                             | 5.5 V           |                       |      | 0.1   |            | 0.1  |      |
|                                 | I <sub>OL</sub> = 24 mA                                     | 4.5 V           |                       |      | 0.36  |            | 0.44 |      |
|                                 |                                                             | 5.5 V           |                       |      | 0.36  |            | 0.44 |      |
|                                 | I <sub>OL</sub> = 50 mA <sup>(1)</sup>                      | 5.5 V           |                       |      |       |            |      |      |
|                                 | I <sub>OL</sub> = 75 mA <sup>(1)</sup>                      | 5.5 V           |                       |      |       |            | 1.65 |      |
| I <sub>OZ</sub>                 | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |      | ±0.25 |            | ±2.5 | µA   |
| I <sub>I</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5.5 V           |                       |      | ±0.1  |            | ±1   | µA   |
| I <sub>CC</sub>                 | V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0 | 5.5 V           |                       |      | 4     |            | 40   | µA   |
| ΔI <sub>CC</sub> <sup>(2)</sup> | One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>  | 5.5 V           |                       | 0.6  |       |            | 1.5  | mA   |
| C <sub>i</sub>                  | V <sub>I</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 4.5  |       |            |      | pF   |
| C <sub>o</sub>                  | V <sub>O</sub> = V <sub>CC</sub> or GND                     | 5 V             |                       | 15   |       |            |      | pF   |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 4.5 Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

|                    |                                 | T <sub>A</sub> = 25°C |     | SN74ACT564 |     | UNIT |
|--------------------|---------------------------------|-----------------------|-----|------------|-----|------|
|                    |                                 | MIN                   | MAX | MIN        | MAX |      |
| f <sub>clock</sub> | Clock frequency                 |                       | 85  |            | 75  | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low | 3                     |     | 3.5        |     | ns   |
| t <sub>su</sub>    | Setup time, data before CLK↑    | 2.5                   |     | 3          |     | ns   |
| t <sub>h</sub>     | Hold time, data after CLK↑      | 1                     |     | 1          |     | ns   |

## 4.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

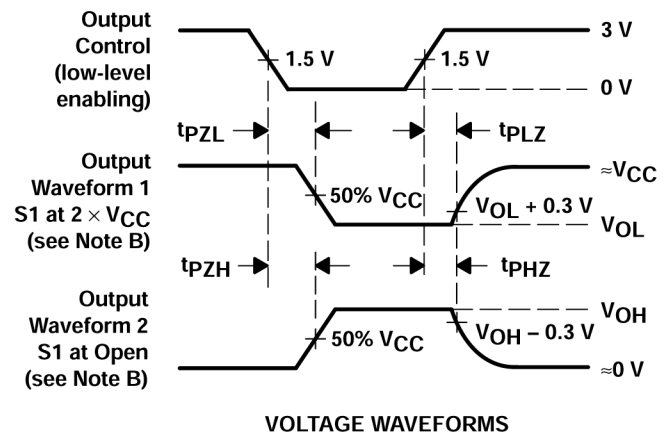
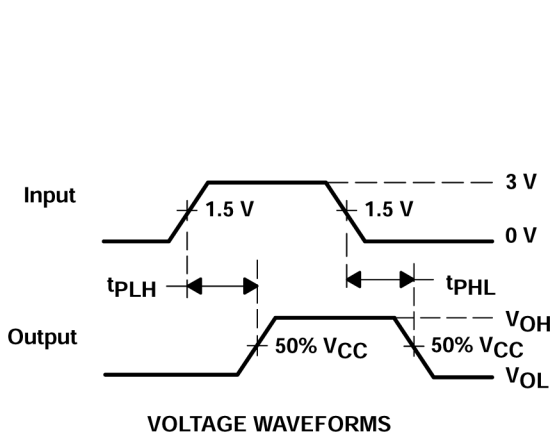
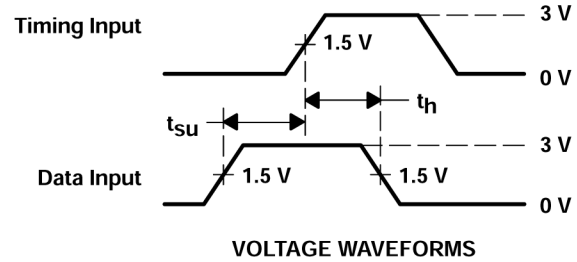
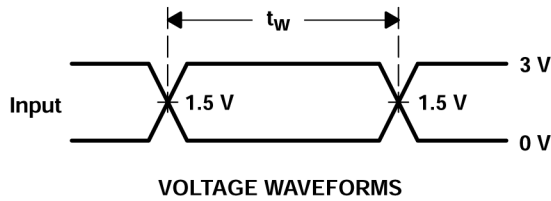
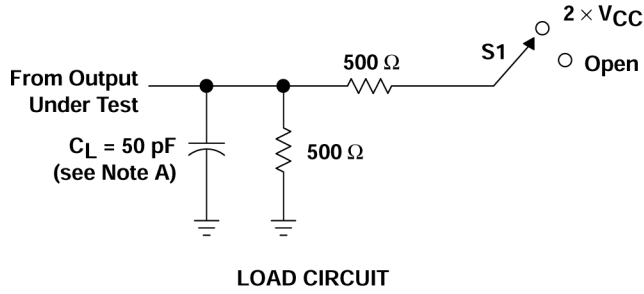
| PARAMETER  | FROM (INPUT)    | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ |     |      | SN74ACT564 |      | UNIT |
|------------|-----------------|-------------|--------------------------|-----|------|------------|------|------|
|            |                 |             | MIN                      | TYP | MAX  | MIN        | MAX  |      |
| $f_{\max}$ |                 |             | 85                       | 90  |      | 75         |      | MHz  |
| $t_{PLH}$  | CLK             | $\bar{Q}$   | 2                        | 6.5 | 10.5 | 1.5        | 11.5 | ns   |
| $t_{PHL}$  |                 |             | 1.5                      | 6   | 9.5  | 1.5        | 10.5 |      |
| $t_{PZH}$  | $\overline{OE}$ | $\bar{Q}$   | 1.5                      | 5.5 | 9    | 1.5        | 9.5  | ns   |
| $t_{PZL}$  |                 |             | 1.5                      | 5.5 | 8.5  | 1          | 9.5  |      |
| $t_{PHZ}$  | $\overline{OE}$ | $\bar{Q}$   | 1.5                      | 7   | 10.5 | 1.5        | 11.5 | ns   |
| $t_{PLZ}$  |                 |             | 1.5                      | 5   | 8    | 1          | 8.5  |      |

## 4.7 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| PARAMETER |                               | TEST CONDITIONS                           | TYP | UNIT |
|-----------|-------------------------------|-------------------------------------------|-----|------|
| $C_{pd}$  | Power dissipation capacitance | $C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$ | 50  | pF   |

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.

**Figure 5-1. Load Circuit and Voltage Waveforms**

| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | Open              |

## 6 Detailed Description

### 6.1 Overview

On the positive transition of the clock (CLK) input, the  $\overline{Q}$  outputs are set to the complements of the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For specified high-impedance state during power up or power down,  $\overline{OE}$  must be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 6.2 Functional Block Diagram

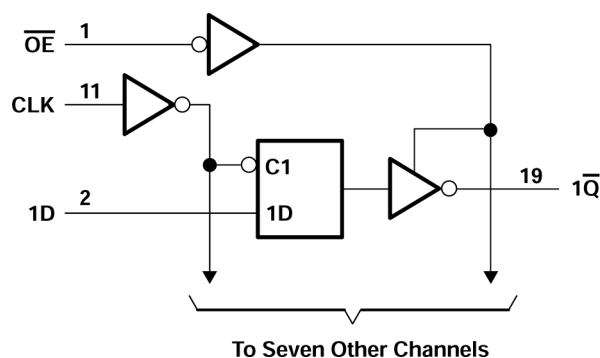


Figure 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

Table 6-1. Function Table (Each Flip-flop)

| INPUTS          |        |   | OUTPUT Q         |
|-----------------|--------|---|------------------|
| $\overline{OE}$ | CLK    | D |                  |
| L               | ↑      | H | L                |
| L               | ↑      | L | H                |
| L               | H or L | X | $\overline{Q}_0$ |
| H               | X      | X | Z                |

## 7 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [Section 4.2](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1  $\mu\text{F}$  and if there are multiple  $V_{CC}$  terminals, then TI recommends .01  $\mu\text{F}$  or .022  $\mu\text{F}$  for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

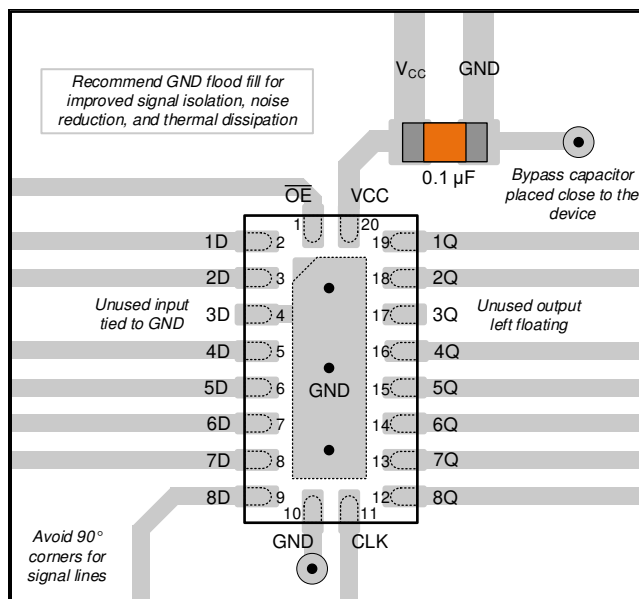
### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

#### 7.2.2 Layout Example



**Figure 7-1. Example layout for the SN74ACT564**

## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS      | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74ACT564 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 8.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 8.6 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Revision C (August 2023) to Revision D (February 2024)</b>                                     | <b>Page</b>       |
|----------------------------------------------------------------------------------------------------------------|-------------------|
| • Added body size to <i>Package Information</i> table .....                                                    | <a href="#">1</a> |
| • Updated R $\theta$ JA values: DW = 58 to 101.2, NS = 60 to 106.2, PW = 83 to 126.2, all values in °C/W ..... | <a href="#">4</a> |

| <b>Changes from Revision B (November 2002) to Revision C (August 2023)</b>                                                                                                                                                                                          | <b>Page</b>       |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| • Added <i>Package Information</i> table, <i>Pin Functions</i> table, <i>Thermal Information</i> table, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section ..... | <a href="#">1</a> |
| • Removed references to SN54ACT564.....                                                                                                                                                                                                                             | <a href="#">1</a> |

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins  | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">SN74ACT564DW</a>  | Obsolete      | Production           | SOIC (DW)   20  | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | ACT564              |
| <a href="#">SN74ACT564DWR</a> | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT564              |
| SN74ACT564DWR.A               | Active        | Production           | SOIC (DW)   20  | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT564              |
| <a href="#">SN74ACT564N</a>   | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ACT564N         |
| SN74ACT564N.A                 | Active        | Production           | PDIP (N)   20   | 20   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | -40 to 85    | SN74ACT564N         |
| <a href="#">SN74ACT564NSR</a> | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-1-260C-UNLIM                | -40 to 85    | ACT564              |
| SN74ACT564NSR.A               | Active        | Production           | SOP (NS)   20   | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | ACT564              |
| <a href="#">SN74ACT564PW</a>  | Obsolete      | Production           | TSSOP (PW)   20 | -                     | -           | Call TI                              | Call TI                           | -40 to 85    | AD564               |
| <a href="#">SN74ACT564PWR</a> | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU   NIPDAU                      | Level-1-260C-UNLIM                | -40 to 85    | AD564               |
| SN74ACT564PWR.A               | Active        | Production           | TSSOP (PW)   20 | 2000   LARGE T&R      | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | AD564               |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ACT564DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ACT564DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.9    | 13.3    | 2.7     | 12.0    | 24.0   | Q1            |
| SN74ACT564NSR | SOP          | NS              | 20   | 2000 | 330.0              | 24.4               | 8.4     | 13.0    | 2.5     | 12.0    | 24.0   | Q1            |
| SN74ACT564PWR | TSSOP        | PW              | 20   | 2000 | 330.0              | 16.4               | 6.95    | 7.0     | 1.4     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ACT564DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ACT564DWR | SOIC         | DW              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ACT564NSR | SOP          | NS              | 20   | 2000 | 356.0       | 356.0      | 45.0        |
| SN74ACT564PWR | TSSOP        | PW              | 20   | 2000 | 353.0       | 353.0      | 32.0        |

## TUBE



\*All dimensions are nominal

| Device        | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|---------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN74ACT564N   | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |
| SN74ACT564N.A | N            | PDIP         | 20   | 20  | 506    | 13.97  | 11230  | 4.32   |



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## NOTES:

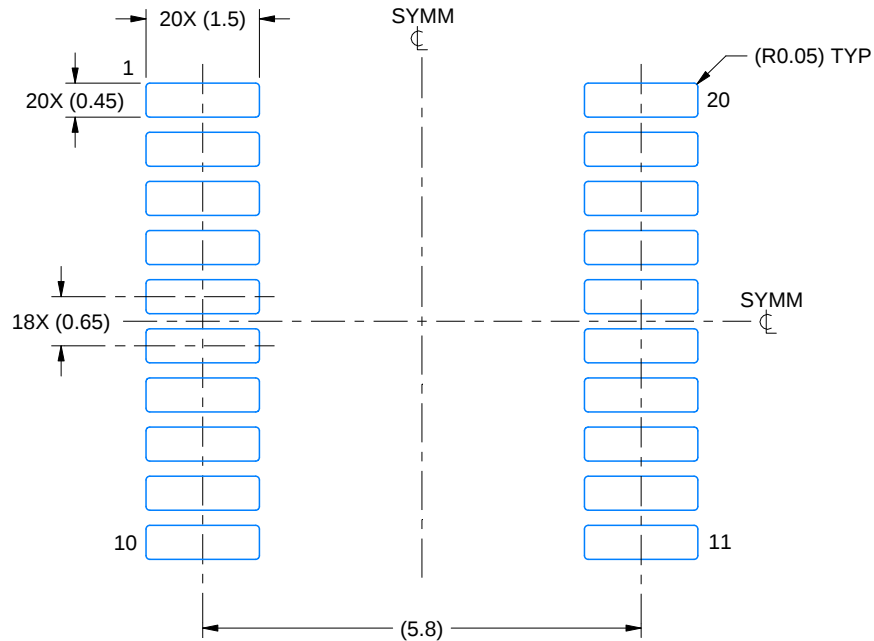
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

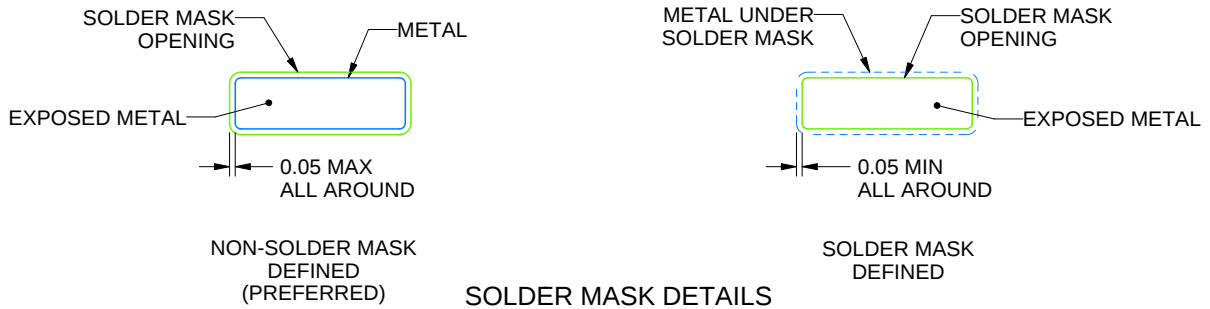
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

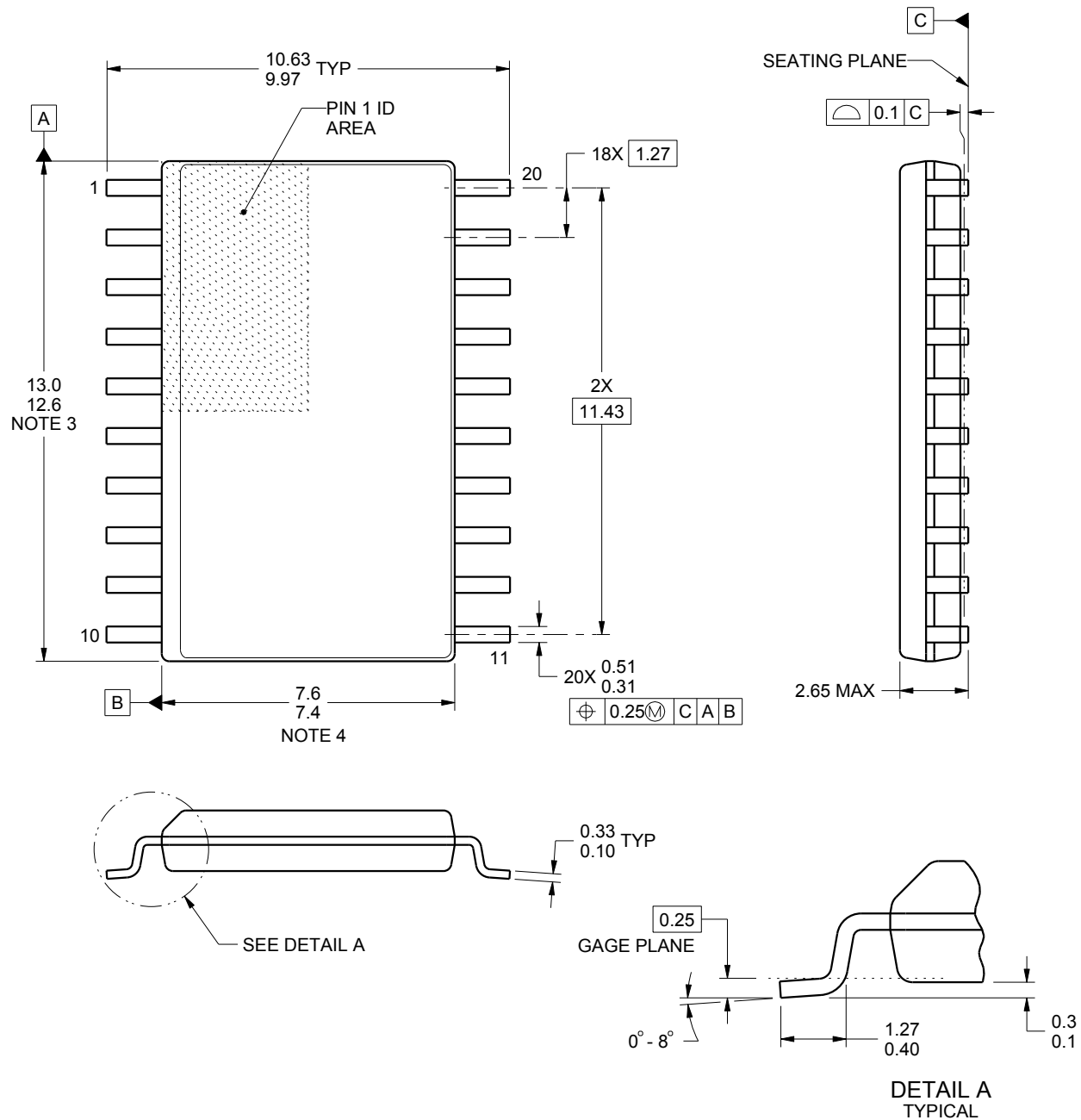
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DW0020A**

## PACKAGE OUTLINE

**SOIC - 2.65 mm max height**

SOIC



4220724/A 05/2016

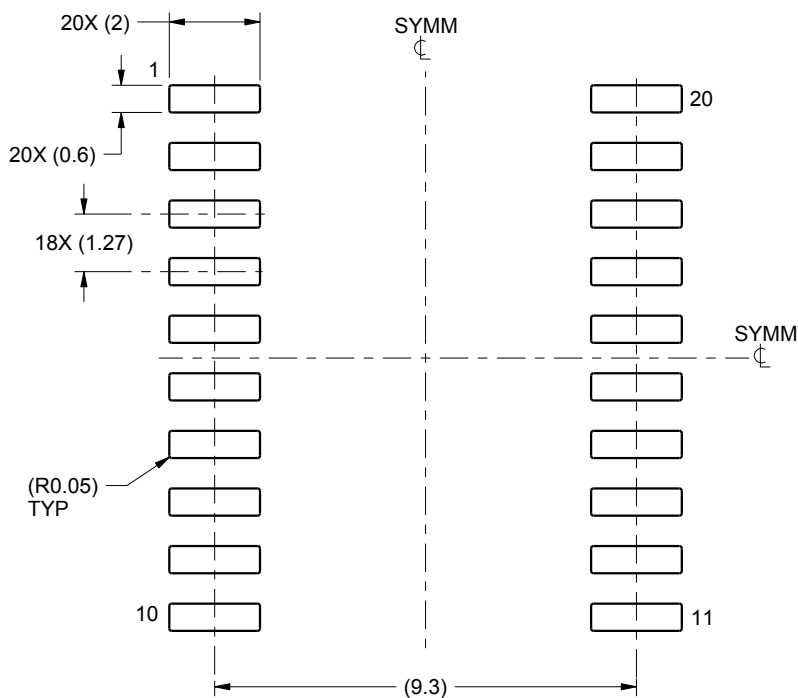
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

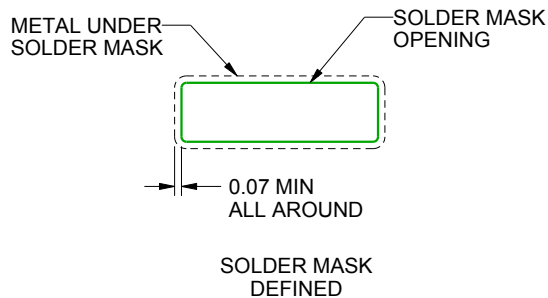
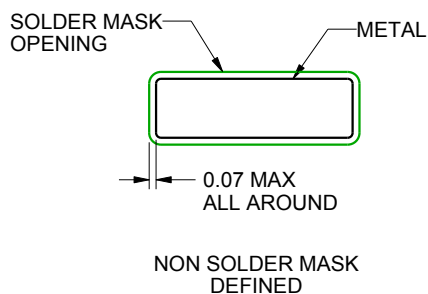
**DW0020A**

### SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



## SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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