# SN74ALVCH162835
# 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

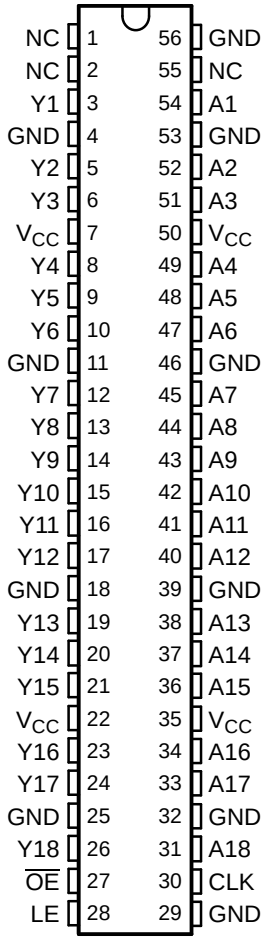
SCES121F–JULY 1997–REVISED OCTOBER 2004

## FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Output Port Has Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages**

NOTE: For tape-and-reel order entry, the DGGR package is abbreviated to GR, and the DGVR package is abbreviated to VR.

**DGG, DGV, OR DL PACKAGE**
**(TOP VIEW)**




NC − No internal connection

## DESCRIPTION

This 18-bit universal bus driver is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

Data flow from A to Y is controlled by the output-enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. When LE is low, the A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch/flip-flop on the low-to-high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

The output port includes equivalent 26-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

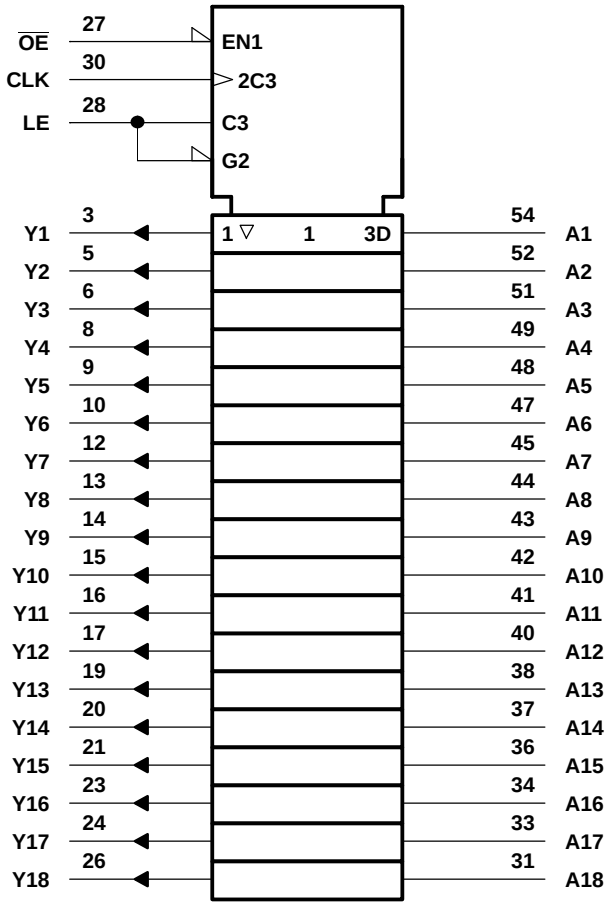
The SN74ALVCH162835 is characterized for operation from -40°C to 85°C.

## FUNCTION TABLE

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OE}$ | LE | CLK | A | Y |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | L | L or H | X | $Y_0$(1) |

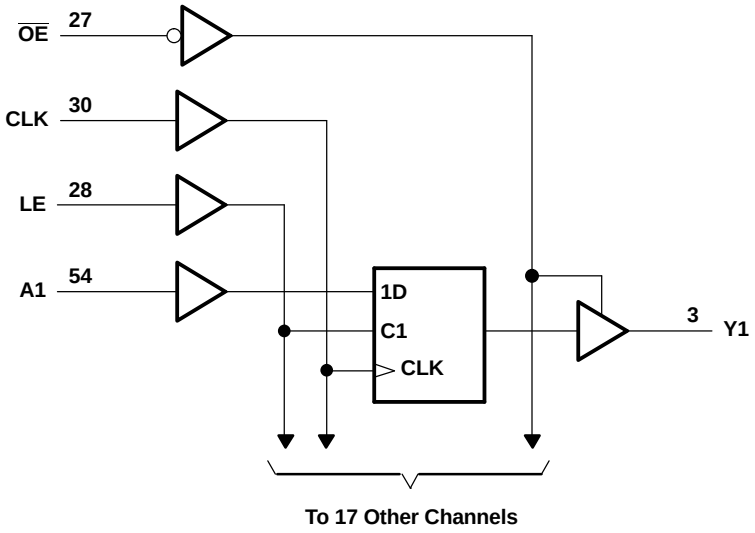
(1) Output level before the indicated steady-state input conditions were established

## LOGIC SYMBOL(1)




(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**LOGIC DIAGRAM (POSITIVE LOGIC)**




## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 4.6 | V |
| $V_I$ | Input voltage range(2) | | -0.5 | 4.6 | V |
| $V_O$ | Output voltage range(2)(3) | | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DGG package | | 81 | °C/W |
| | | DGV package | | 86 | |
| | | DL package | | 74 | |
| $T_{stg}$ | Storage temperature range | | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

## RECOMMENDED OPERATING CONDITIONS(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | $0.65 \times V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | $0.35 \times V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | -2 | mA |
| | | $V_{CC}$ = 2.3 V | | -6 | |
| | | $V_{CC}$ = 2.7 V | | -8 | |
| | | $V_{CC}$ = 3 V | | -12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 2 | mA |
| | | $V_{CC}$ = 2.3 V | | 6 | |
| | | $V_{CC}$ = 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | | $I_{OH}$ = -100 μA | 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | | | V |
| | | $I_{OH}$ = -2 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = -4 mA | 2.3 V | 1.9 | | | |
| | | $I_{OH}$ = -6 mA | 2.3 V | 1.7 | | | |
| | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = -8 mA | 2.7 V | 2 | | | |
| | | $I_{OH}$ = -12 mA | 3 V | 2 | | | |
| $V_{OL}$ | | $I_{OL}$ = 100 μA | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 2 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 4 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 2.3 V | | | 0.55 | |
| | | | 3 V | | | 0.55 | |
| | | $I_{OL}$ = 8 mA | 2.7 V | | | 0.6 | |
| | | $I_{OL}$ = 12 mA | 3 V | | | 0.8 | |
| $I_I$ | | $V_I$ = $V_{CC}$ or GND | 3.6 V | | | ±5 | μA |
| $I_{I(hold)}$ | | $V_I$ = 0.58 V | 1.65 V | 25 | | | μA |
| | | $V_I$ = 1.07 V | 1.65 V | -25 | | | |
| | | $V_I$ = 0.7 V | 2.3 V | 45 | | | |
| | | $V_I$ = 1.7 V | 2.3 V | -45 | | | |
| | | $V_I$ = 0.8 V | 3 V | 75 | | | |
| | | $V_I$ = 2 V | 3 V | -75 | | | |
| | | $V_I$ = 0 to 3.6 V(2) | 3.6 V | | | ±500 | |
| $I_{OZ}$ | | $V_O$ = $V_{CC}$ or GND | 3.6 V | | | ±10 | μA |
| $I_{CC}$ | | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 40 | μA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ - 0.6 V, Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | μA |
| $C_i$ | Control inputs | $V_I$ = $V_{CC}$ or GND | 3.3 V | | 3.5 | | pF |
| | Data inputs | | | | 6 | | |
| $C_o$ | Outputs | $V_O$ = $V_{CC}$ or GND | 3.3 V | | 7 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| | | | | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | | (1) | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration | LE high | | (1) | | 3.3 | | 3.3 | | 3.3 | | ns |
| | | CLK high or low | | (1) | | 3.3 | | 3.3 | | 3.3 | | |
| $t_{su}$ | Setup time | Data before CLK↑ | | (1) | | 2.2 | | 2.1 | | 1.7 | | ns |
| | | Data before LE↓ | CLK high | (1) | | 1.9 | | 1.6 | | 1.5 | | |
| | | | CLK low | (1) | | 1.3 | | 1.1 | | 1 | | |
| $t_h$ | Hold time | Data after CLK↑ | | (1) | | 0.6 | | 0.6 | | 0.7 | | ns |
| | | Data after LE↓ | CLK high or low | (1) | | 1.4 | | 1.7 | | 1.4 | | |

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | (1) | | 150 | | 150 | | 150 | | MHz |
| $t_{pd}$ | A | Y | | (1) | 1 | 5 | | 5 | 1 | 4.2 | ns |
| | LE | | | (1) | 1.3 | 5.9 | | 5.8 | 1.3 | 5.1 | |
| | CLK | | | (1) | 1.4 | 6.3 | | 6.1 | 1.4 | 5.4 | |
| $t_{en}$ | $\overline{OE}$ | Y | | (1) | 1.4 | 6.3 | | 6.5 | 1.1 | 5.5 | ns |
| $t_{dis}$ | $\overline{OE}$ | Y | | (1) | 1 | 4.7 | | 4.9 | 1.3 | 4.5 | ns |

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

from 0°C to 65°C, $C_L$ = 50 pF

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.15 V | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $t_{pd}$ | CLK | Y | 1.9 | 5 | ns |

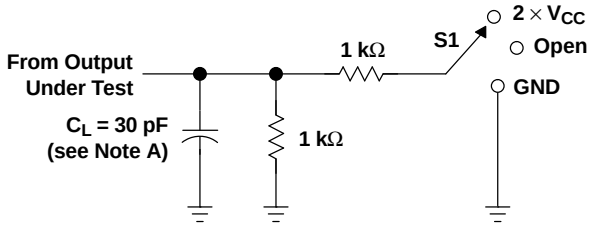
## OPERATING CHARACTERISTICS

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | Outputs enabled | $C_L$ = 0, f = 10 MHz | (1) | 36 | 41 | pF |
| | | Outputs disabled | | (1) | 12.5 | 14 | |

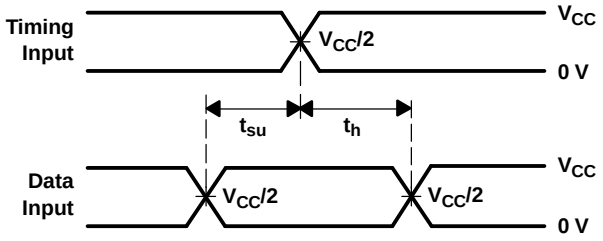
(1) This information was not available at the time of publication.

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V

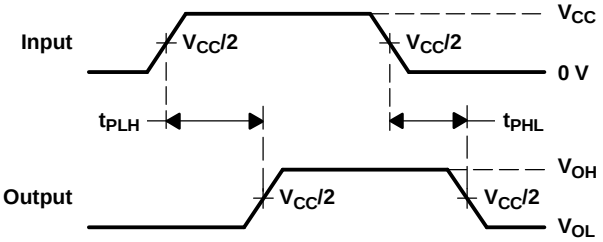



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

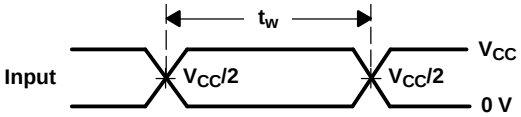
LOAD CIRCUIT



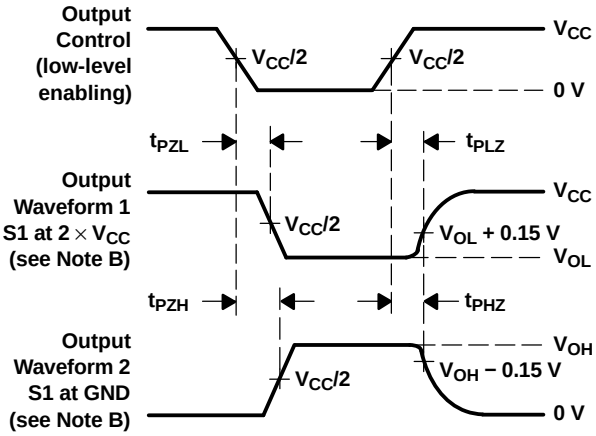

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

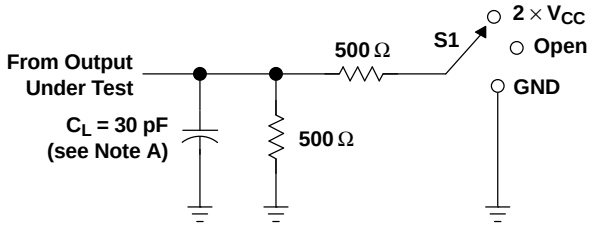



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

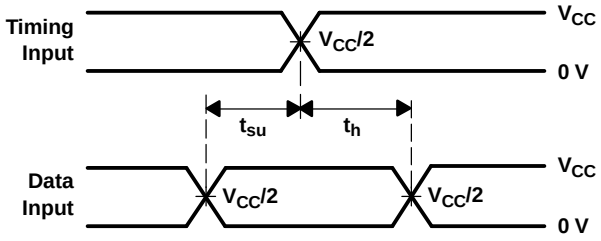
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASURE INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

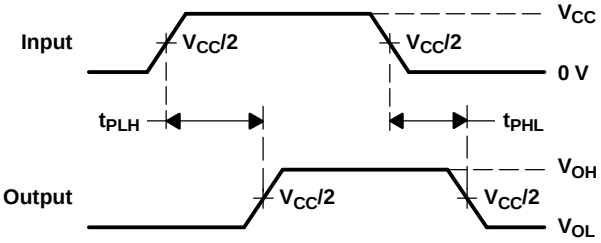



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

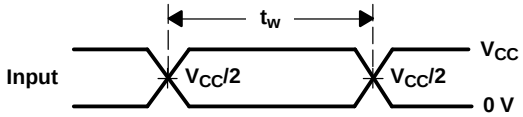
LOAD CIRCUIT



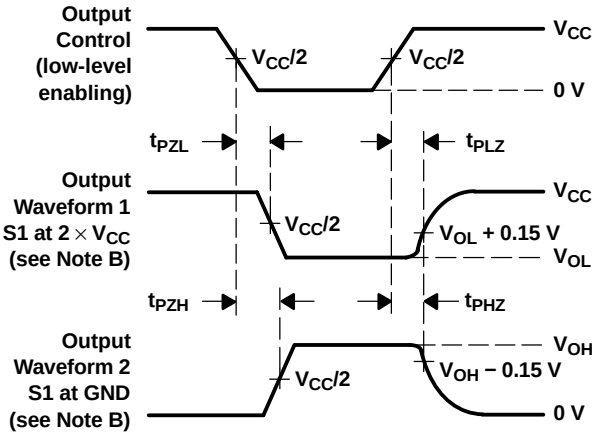

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

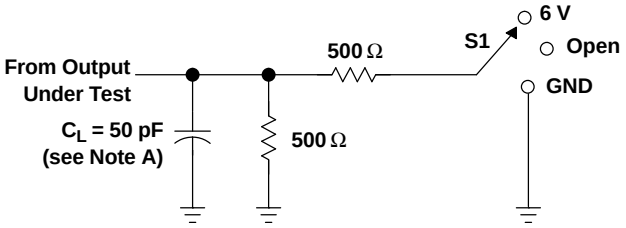



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

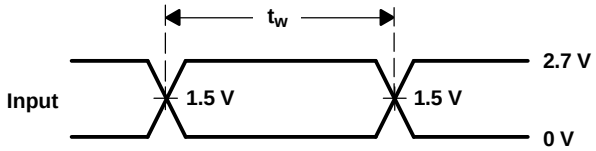
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASURE INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

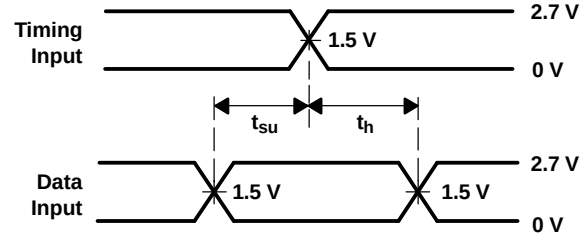



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

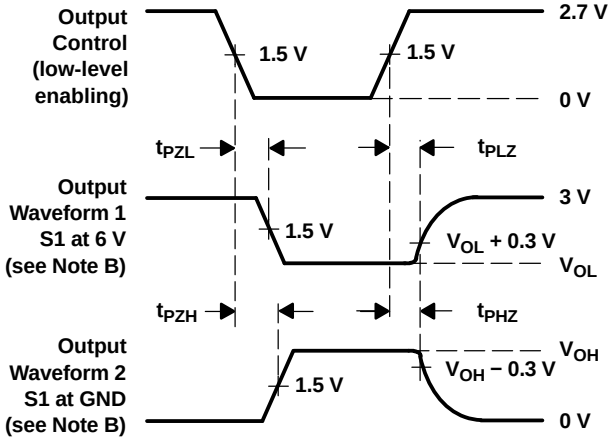
LOAD CIRCUIT



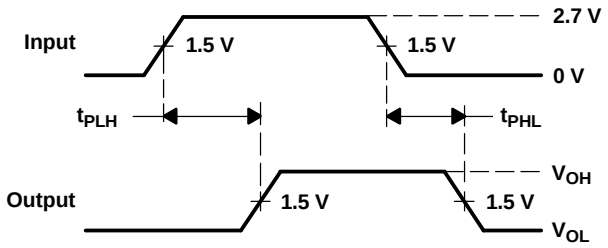

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| 74ALVCH162835DLG4 | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162835DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162835GRE4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162835GRG4 | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162835VRE4 | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ALVCH162835VRG4 | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162835DGGR | OBSOLETE | TSSOP | DGG | 56 | | TBD | Call TI | Call TI |
| SN74ALVCH162835DGVR | OBSOLETE | TVSOP | DGV | 56 | | TBD | Call TI | Call TI |
| SN74ALVCH162835DL | ACTIVE | SSOP | DL | 56 | 20 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162835DLR | ACTIVE | SSOP | DL | 56 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162835GR | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ALVCH162835VR | ACTIVE | TVSOP | DGV | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

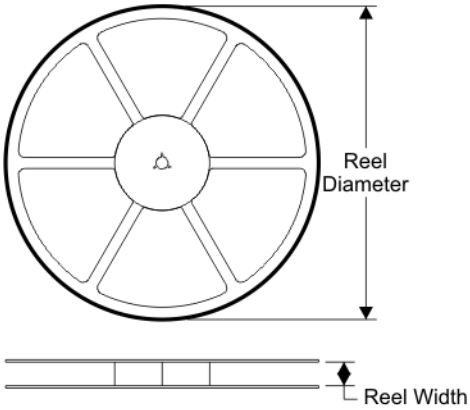
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

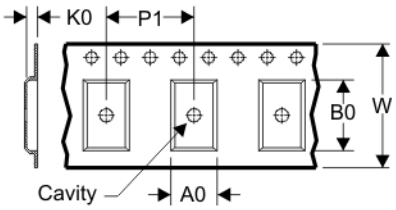
to Customer on an annual basis.

## TAPE AND REEL BOX INFORMATION

**REEL DIMENSIONS**

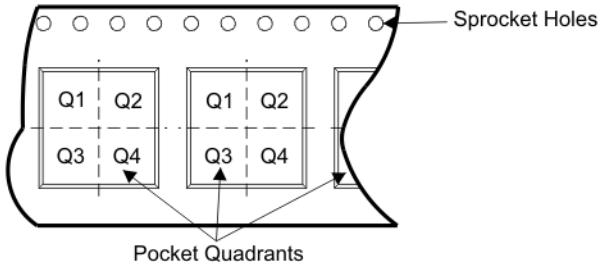



**TAPE DIMENSIONS**



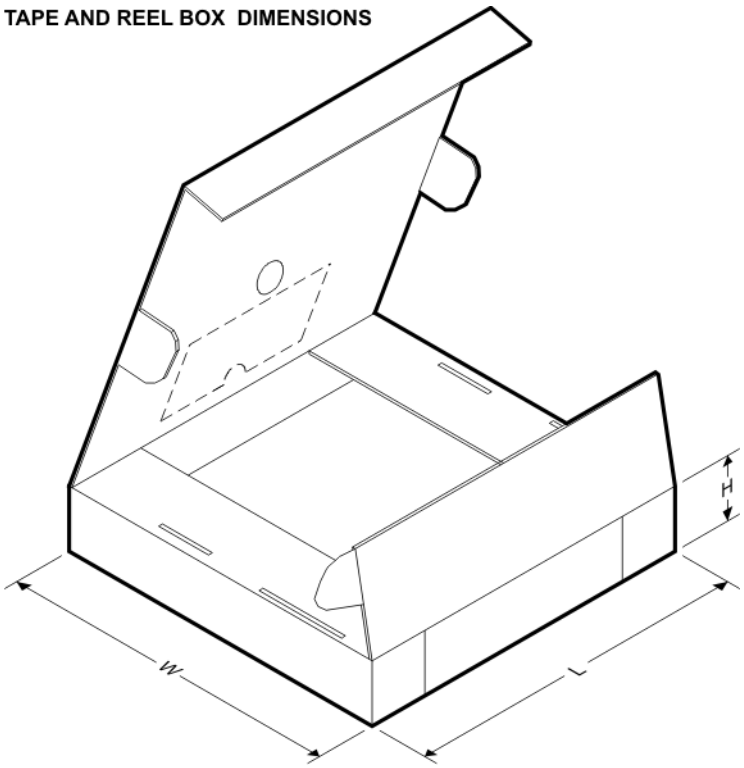

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALVCH162835DLR | DL | 56 | SITE 41 | 330 | 32 | 11.35 | 18.67 | 3.1 | 16 | 32 | Q1 |
| SN74ALVCH162835GR | DGG | 56 | SITE 41 | 330 | 24 | 8.6 | 15.6 | 1.8 | 12 | 24 | Q1 |
| SN74ALVCH162835VR | DGV | 56 | SITE 41 | 330 | 24 | 6.8 | 11.7 | 1.6 | 12 | 24 | Q1 |

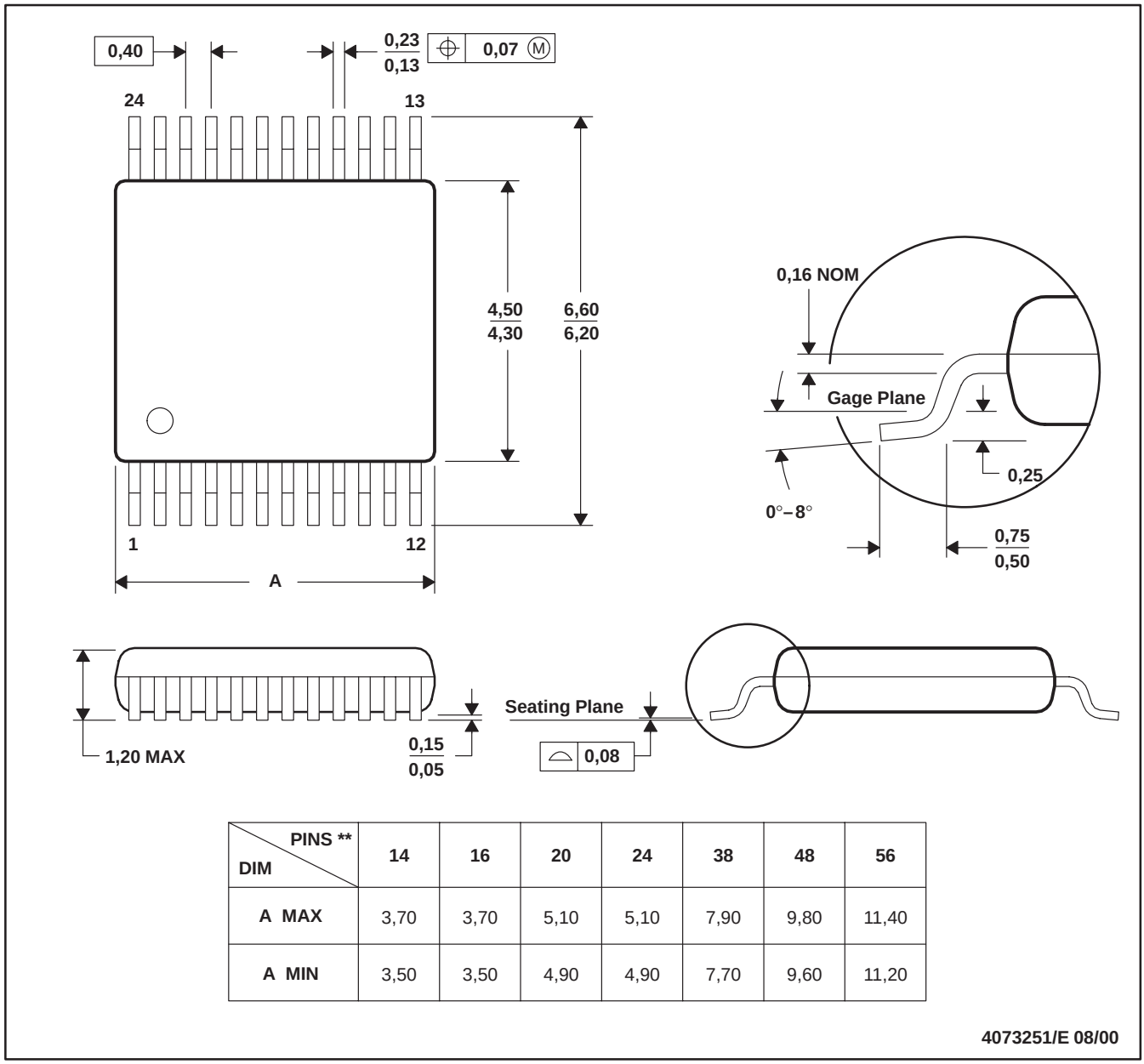
TAPE AND REEL BOX DIMENSIONS




| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| SN74ALVCH162835DLR | DL | 56 | SITE 41 | 346.0 | 346.0 | 49.0 |
| SN74ALVCH162835GR | DGG | 56 | SITE 41 | 346.0 | 346.0 | 41.0 |
| SN74ALVCH162835VR | DGV | 56 | SITE 41 | 346.0 | 346.0 | 41.0 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**



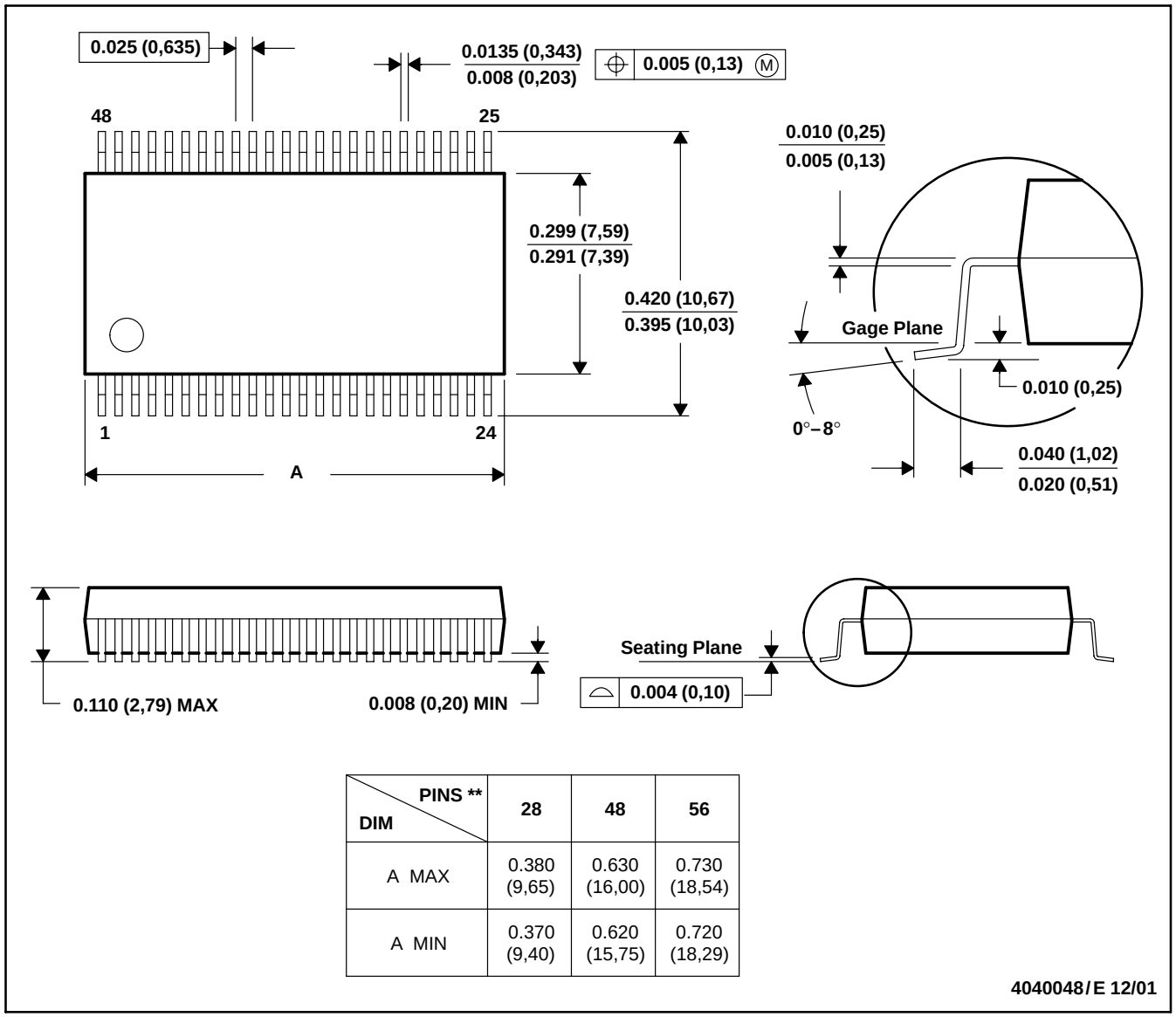

| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

**DL (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**



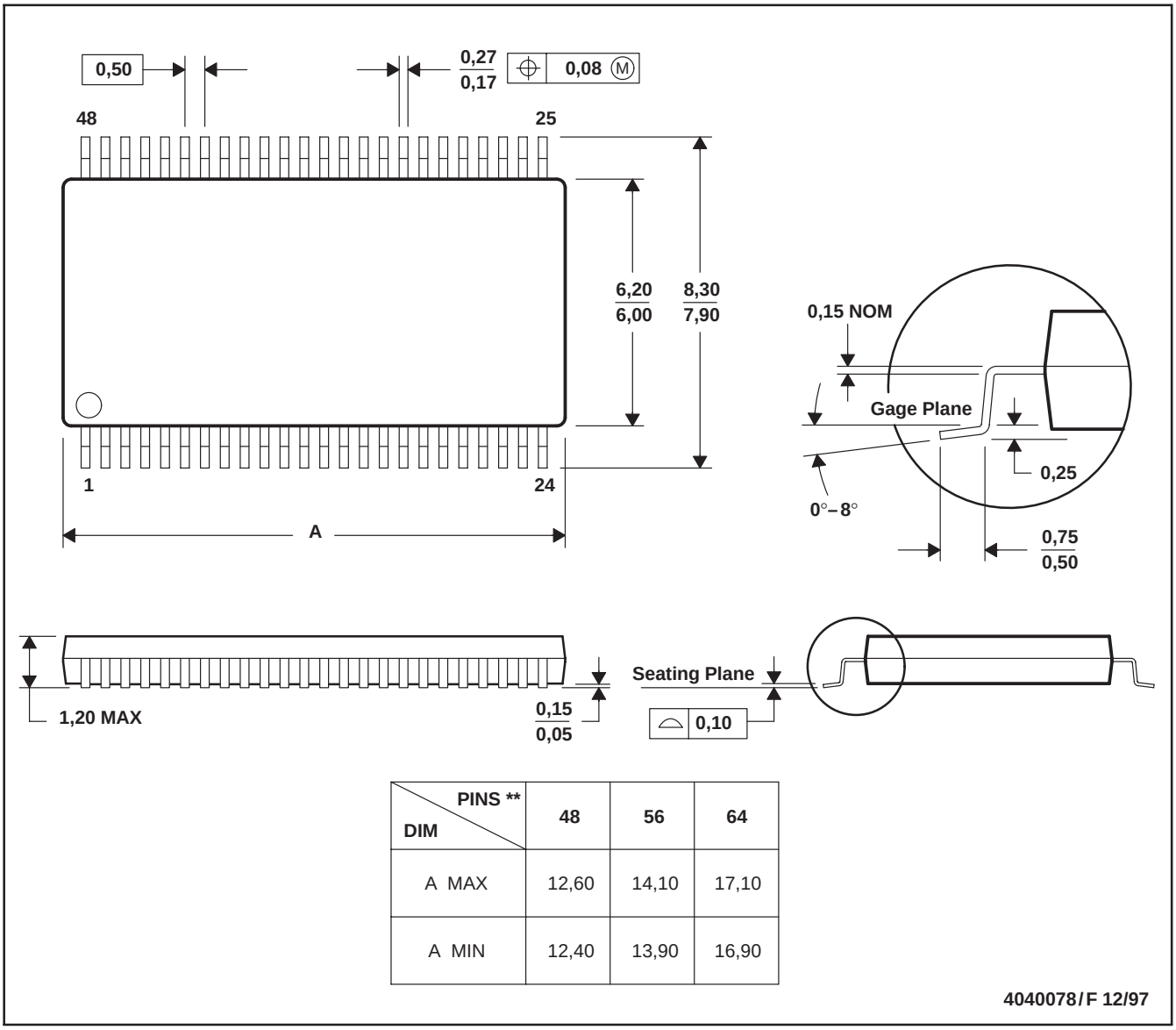

| DIM \ PINS ** | 28 | 48 | 56 |
|---|---|---|---|
| A MAX | 0.380 (9,65) | 0.630 (16,00) | 0.730 (18,54) |
| A MIN | 0.370 (9,40) | 0.620 (15,75) | 0.720 (18,29) |

**4040048/E 12/01**

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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