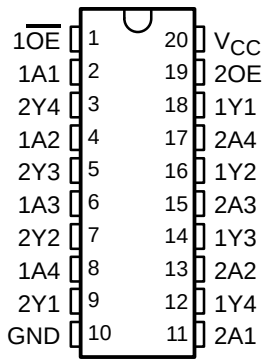
- **Operating Voltage Range of 4.5 V to 5.5 V**
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required**
- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**

DW, N OR NS PACKAGE
(TOP VIEW)



description/ordering information

This SN74BCT2241 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the ’BCT2240 and ’BCT2244 devices, this device provides the choice of selected combinations of inverting and noninverting outputs, symmetrical active-low output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs. This device features high fan-out and improved fan-in.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

The outputs, which are designed to source or sink up to 12 mA, include 33-Ω series resistors to reduce overshoot and undershoot.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74BCT2241N	SN74BCT2241N
	SOIC – DW	Tube	SN74BCT2241DW	BCT2241
		Tape and reel	SN74BCT2241DWR	
	SOP – NS	Tape and reel	SN74BCT2241NSR	BCT2241

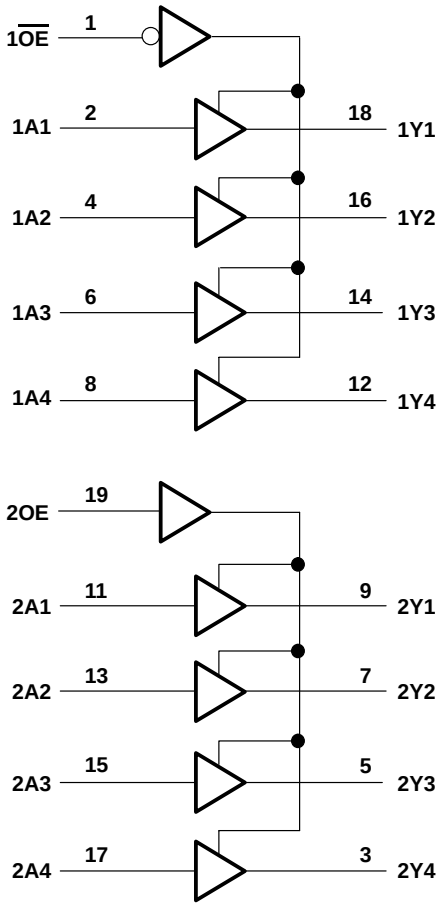
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLES

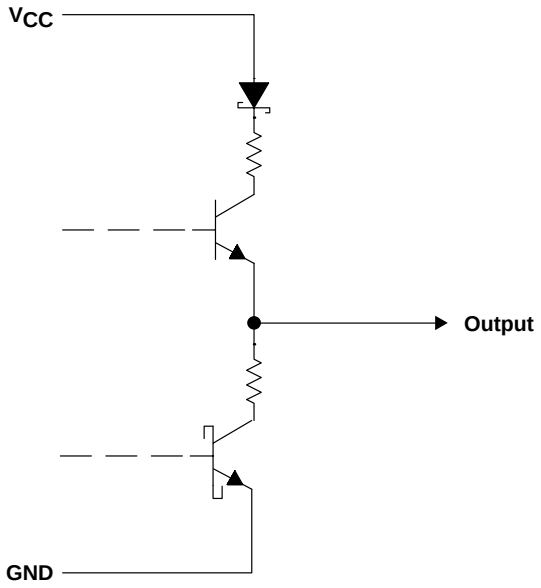
INPUTS		OUTPUT
$1\overline{OE}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic diagram (positive logic)



schematic of Y outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . –0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . –0.5 V to V_{CC}
Input clamp current, I_{IK} . . . . . –30 mA
Current into any output in the low state, I_O . . . . . 24 mA
Package thermal impedance, θ_{JA} (see Note 2): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	0		70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

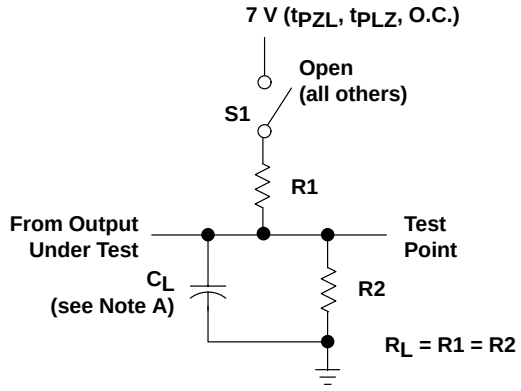
PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4	3.3		V
		I_{OH} = –12 mA	2			
	V_{CC} = 4.75 V,	I_{OH} = –3 mA	2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 1 mA		0.15	0.5	V
		I_{OL} = 12 mA		0.42	0.8	
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			–1	mA
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			–50	µA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–100		–225	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		23	37	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		48	76	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		6	9	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V		6		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V		11		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

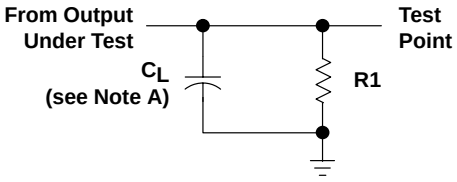
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.1	3	4.4	1.1	4.9	ns
t_{PHL}			2.9	4.9	6.6	2.9	6.9	
t_{PZH}	OE or $\overline{OE}$	Y	2.7	6	7.8	2.7	8.9	ns
t_{PZL}			4.1	7.7	9.4	4.1	10.3	
t_{PHZ}	OE or $\overline{OE}$	Y	2.5	5.2	7.2	2.5	8.7	ns
t_{PLZ}			3.2	7.1	9.5	3.2	11.3	

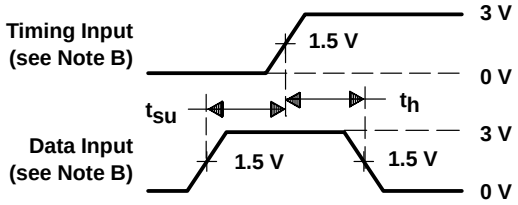
PARAMETER MEASUREMENT INFORMATION



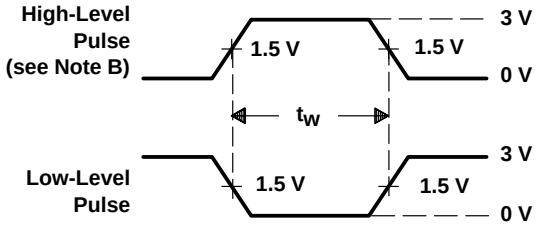
LOAD CIRCUIT FOR
3-STATE AND OPEN-COLLECTOR OUTPUTS



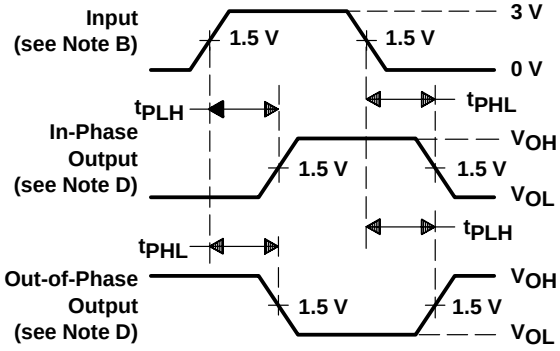
LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS



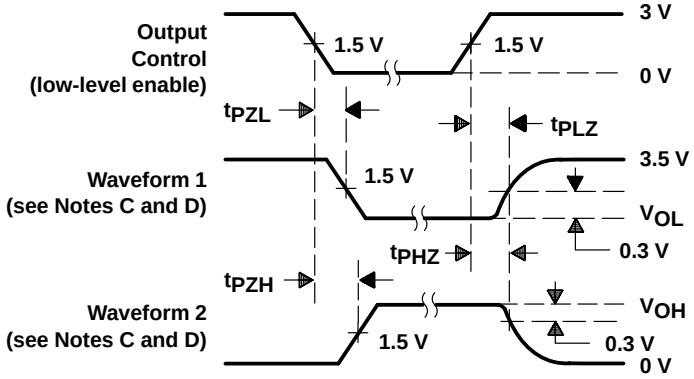
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (see Note D)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

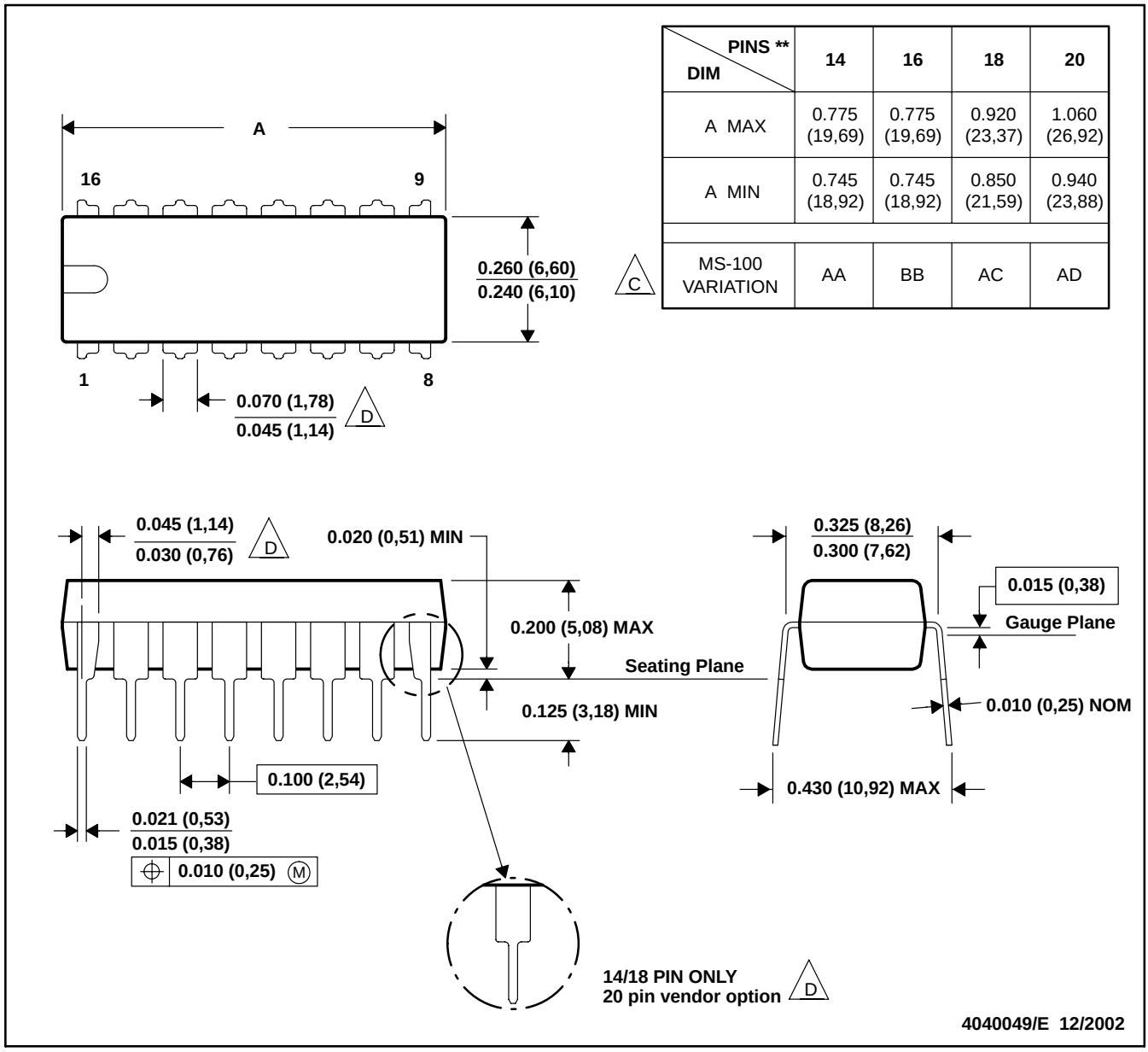
NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $t_r = t_f \leq 2.5$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.
F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-100 VARIATION	AA	BB	AC	AD

NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body lrngth (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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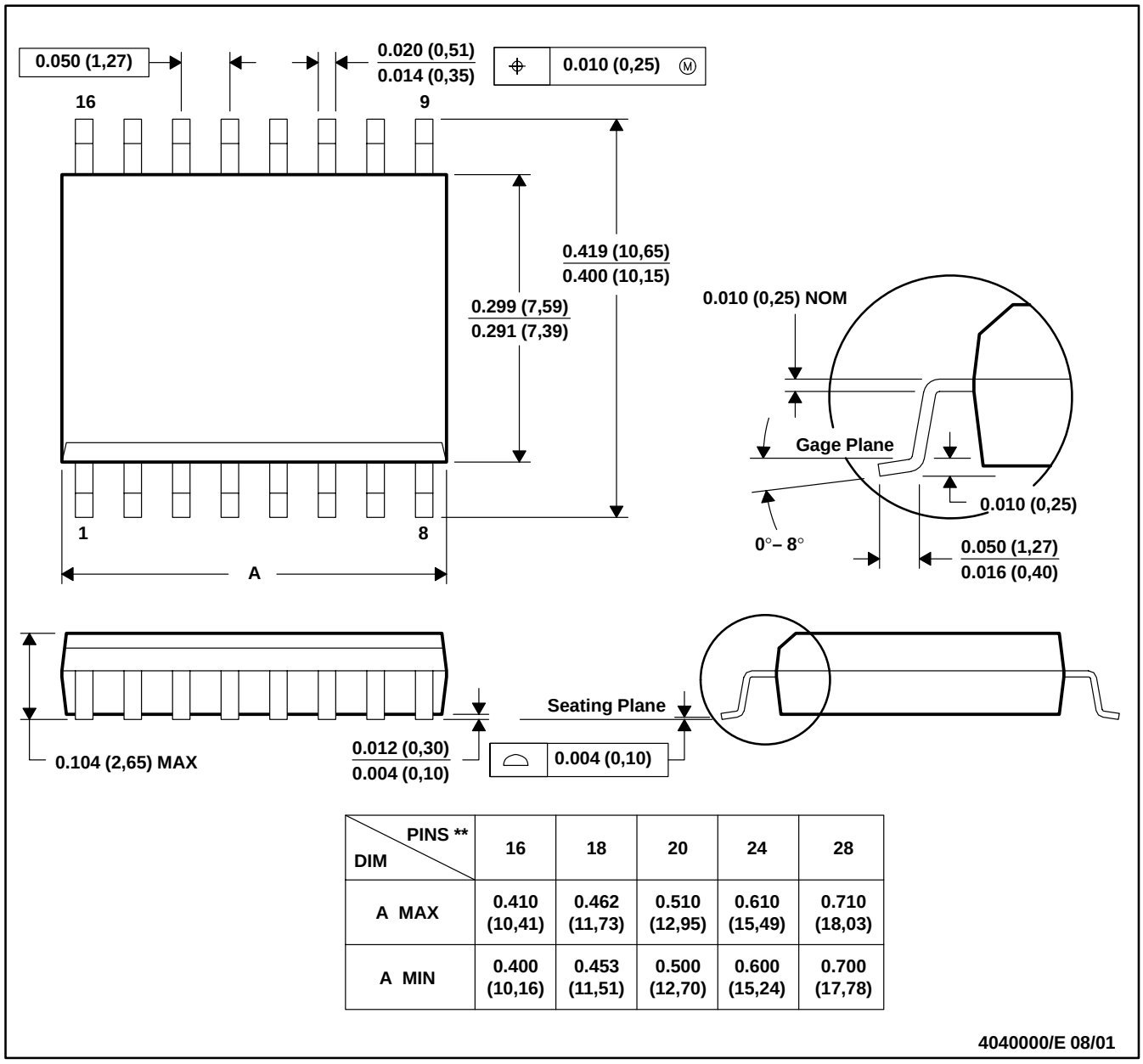
DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PINS SHOWN



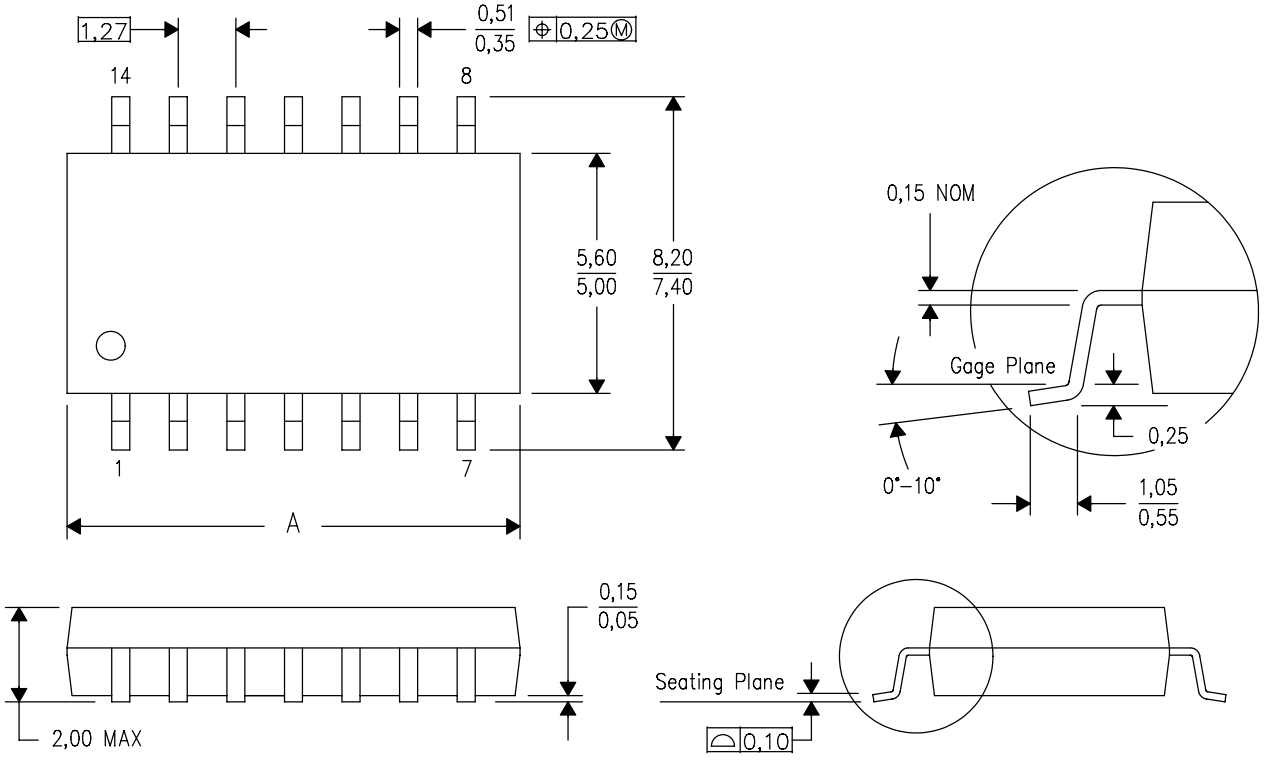
DIM \ PINS **	16	18	20	24	28
A MAX	0.410 (10,41)	0.462 (11,73)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.453 (11,51)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4040000/E 08/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

NS (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

14–PIN SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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