

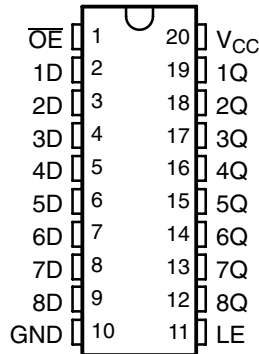
# SN54BCT573, SN74BCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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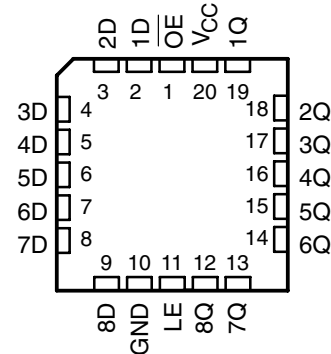
- Operating Voltage Range of 4.5 V to 5.5 V
- State-of-the-Art BiCMOS Design Significantly Reduces  $I_{CCZ}$
- Full Parallel Access for Loading

- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

SN54BCT573 ... J OR W PACKAGE  
SN74BCT573 ... DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54BCT573 ... FK PACKAGE  
(TOP VIEW)



## description/ordering information

These 8-bit latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the 'BCT573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels that were set up at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$  does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

## ORDERING INFORMATION

| $T_A$          | PACKAGE†  |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-----------|---------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP – N  | Tube          | SN74BCT573N           | SN74BCT573N      |
|                | SOIC – DW | Tube          | SN74BCT573DW          | BCT573           |
|                |           | Tape and reel | SN74BCT573DWR         |                  |
|                | SOP – NS  | Tape and reel | SN74BCT573NSR         | BCT573           |
| –55°C to 125°C | CDIP – J  | Tube          | SNJ54BCT573J          | SNJ54BCT573J     |
|                | CFP – W   | Tube          | SNJ54BCT573W          | SNJ54BCT573W     |
|                | LCCC – FK | Tube          | SNJ54BCT573FK         | SNJ54BCT573FK    |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

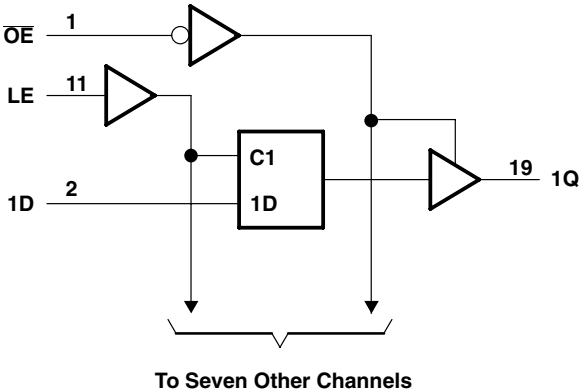
# SN54BCT573, SN74BCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each latch)

| INPUTS |    |   | OUTPUT<br>Q    |
|--------|----|---|----------------|
| OE     | LE | D |                |
| L      | H  | H | H              |
| L      | H  | L | L              |
| L      | L  | X | Q <sub>0</sub> |
| H      | X  | X | Z              |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|                                                                                        |                           |
|----------------------------------------------------------------------------------------|---------------------------|
| Supply voltage range, V <sub>CC</sub>                                                  | –0.5 V to 7 V             |
| Input voltage range, V <sub>I</sub> (see Note 1)                                       | –0.5 V to 7 V             |
| Voltage range applied to any output in the disabled or power-off state, V <sub>O</sub> | –0.5 V to 5.5 V           |
| Voltage range applied to any output in the high state, V <sub>O</sub>                  | –0.5 V to V <sub>CC</sub> |
| Input clamp current, I <sub>IK</sub> (V <sub>I</sub> < 0)                              | –30 mA                    |
| Current into any output in the low state: SN54BCT573                                   | 96 mA                     |
| SN74BCT573                                                                             | 128 mA                    |
| Package thermal impedance, θ <sub>JA</sub> (see Note 2): DW package                    | 58°C/W                    |
| N package                                                                              | 69°C/W                    |
| NS package                                                                             | 60°C/W                    |
| Storage temperature range, T <sub>stg</sub>                                            | –65°C to 150°C            |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

# SN54BCT573, SN74BCT573 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 3)

|          |                                | SN54BCT573 |     |     | SN74BCT573 |     |     | UNIT |
|----------|--------------------------------|------------|-----|-----|------------|-----|-----|------|
|          |                                | MIN        | NOM | MAX | MIN        | NOM | MAX |      |
| $V_{CC}$ | Supply voltage                 | 4.5        | 5   | 5.5 | 4.5        | 5   | 5.5 | V    |
| $V_{IH}$ | High-level input voltage       | 2          |     |     | 2          |     |     | V    |
| $V_{IL}$ | Low-level input voltage        |            |     | 0.8 |            |     | 0.8 | V    |
| $I_{IK}$ | Input clamp current            |            |     | -18 |            |     | -18 | mA   |
| $I_{OH}$ | High-level output current      |            |     | -12 |            |     | -15 | mA   |
| $I_{OL}$ | Low-level output current       |            |     | 48  |            |     | 64  | mA   |
| $T_A$    | Operating free-air temperature | -55        |     | 125 | 0          |     | 70  | °C   |

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                                                   |                          | SN54BCT573 |      |      | SN74BCT573 |      |      | UNIT |
|-------------------|-------------------------------------------------------------------|--------------------------|------------|------|------|------------|------|------|------|
|                   |                                                                   |                          | MIN        | TYP† | MAX  | MIN        | TYP† | MAX  |      |
| $V_{IK}$          | $V_{CC} = 4.5\text{ V}$ ,<br>$I_I = -18\text{ mA}$                |                          |            |      | -1.2 |            |      | -1.2 | V    |
| $V_{OH}$          | $V_{CC} = 4.5\text{ V}$                                           | $I_{OH} = -3\text{ mA}$  | 2.4        | 3.3  |      | 2.4        | 3.3  |      | V    |
|                   |                                                                   | $I_{OH} = -12\text{ mA}$ | 2          | 3.2  |      |            |      |      |      |
|                   |                                                                   | $I_{OH} = -15\text{ mA}$ |            |      |      | 2          | 3.1  |      |      |
| $V_{OL}$          | $V_{CC} = 4.5\text{ V}$                                           | $I_{OL} = 48\text{ mA}$  |            | 0.38 | 0.55 |            |      |      | V    |
|                   |                                                                   | $I_{OL} = 64\text{ mA}$  |            |      |      |            | 0.42 | 0.55 |      |
| $I_I$             | $V_{CC} = 5.5\text{ V}$ ,<br>$V_I = 5.5\text{ V}$                 |                          |            |      | 0.4  |            |      | 0.4  | mA   |
| $I_{IH}$          | $V_{CC} = 5.5\text{ V}$ ,<br>$V_I = 2.7\text{ V}$                 |                          |            |      | 20   |            |      | 20   | μA   |
| $I_{IL}$          | $V_{CC} = 5.5\text{ V}$ ,<br>$V_I = 0.5\text{ V}$                 |                          |            |      | -0.6 |            |      | -0.6 | mA   |
| $I_{OS}^\ddagger$ | $V_{CC} = 5.5\text{ V}$ ,<br>$V_O = 0$                            |                          | -100       |      | -225 | -100       |      | -225 | mA   |
| $I_{OZH}$         | $V_{CC} = 5.5\text{ V}$ ,<br>$V_O = 2.7\text{ V}$                 |                          |            |      | 50   |            |      | 50   | μA   |
| $I_{OZL}$         | $V_{CC} = 5.5\text{ V}$ ,<br>$V_O = 0.5\text{ V}$                 |                          |            |      | -50  |            |      | -50  | μA   |
| $I_{CCL}$         | $V_{CC} = 5.5\text{ V}$ ,<br>Outputs open                         |                          |            |      | 62   |            |      | 62   | mA   |
| $I_{CCH}$         | $V_{CC} = 5.5\text{ V}$ ,<br>Outputs open                         |                          |            |      | 8    |            |      | 8    | mA   |
| $I_{CCZ}$         | $V_{CC} = 5.5\text{ V}$ ,<br>Outputs open                         |                          |            |      | 8    |            |      | 8    | mA   |
| $C_i$             | $V_{CC} = 5\text{ V}$ ,<br>$V_I = 2.5\text{ V}$ or $0.5\text{ V}$ |                          |            | 5.5  |      |            | 5.5  |      | pF   |
| $C_o$             | $V_{CC} = 5\text{ V}$ ,<br>$V_O = 2.5\text{ V}$ or $0.5\text{ V}$ |                          |            | 7.5  |      |            | 7.5  |      | pF   |

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

|          |                             | $V_{CC} = 5\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$ |     | SN54BCT573 |     | SN74BCT573 |     | UNIT |
|----------|-----------------------------|-----------------------------------------------------|-----|------------|-----|------------|-----|------|
|          |                             | MIN                                                 | MAX | MIN        | MAX | MIN        | MAX |      |
| $t_w$    | Pulse duration, LE high     | 4                                                   |     | 4          |     | 4          |     | ns   |
| $t_{su}$ | Setup time, data before LE↓ | 1                                                   |     | 2.5        |     | 1          |     | ns   |
| $t_h$    | Hold time, data after LE↓   | 4                                                   |     | 4          |     | 4          |     | ns   |



# SN54BCT573, SN74BCT573

## OCTAL TRANSPARENT D-TYPE LATCHES

### WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 5$ V,<br>$T_A = 25^\circ\text{C}$ |     |     | SN54BCT573 |      | SN74BCT573 |      | UNIT |
|-----------|-----------------|----------------|---------------------------------------------|-----|-----|------------|------|------------|------|------|
|           |                 |                | MIN                                         | TYP | MAX | MIN        | MAX  | MIN        | MAX  |      |
| $t_{PLH}$ | D               | Q              | 2                                           | 5   | 7.2 | 1          | 9.8  | 2          | 8.4  | ns   |
| $t_{PHL}$ |                 |                | 2.8                                         | 5.9 | 8.2 | 1.5        | 10.3 | 2.8        | 9.6  |      |
| $t_{PLH}$ | LE              | Q              | 2.4                                         | 6.1 | 7.2 | 2          | 9.7  | 2.4        | 8.1  | ns   |
| $t_{PHL}$ |                 |                | 2.9                                         | 5.2 | 7.1 | 2          | 8.8  | 2.9        | 7.8  |      |
| $t_{PZH}$ | $\overline{OE}$ | Q              | 3                                           | 6.2 | 8.5 | 2.5        | 11   | 3          | 10.4 | ns   |
| $t_{PZL}$ |                 |                | 4.3                                         | 7.1 | 9.3 | 3.5        | 11.5 | 4.3        | 11   |      |
| $t_{PHZ}$ | $\overline{OE}$ | Q              | 2.2                                         | 3.9 | 5.6 | 1.5        | 7.2  | 2.2        | 6    | ns   |
| $t_{PLZ}$ |                 |                | 1.7                                         | 3.6 | 5.2 | 1          | 7    | 1.7        | 6    |      |

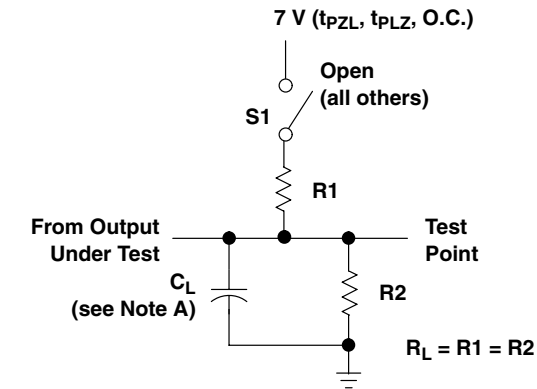


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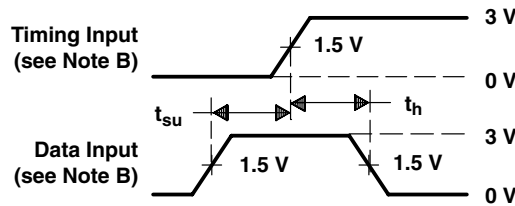
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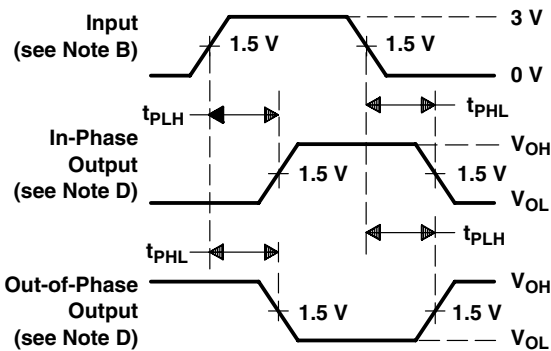
## PARAMETER MEASUREMENT INFORMATION



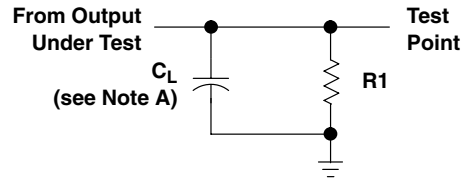
LOAD CIRCUIT FOR  
3-STATE AND OPEN-COLLECTOR OUTPUTS



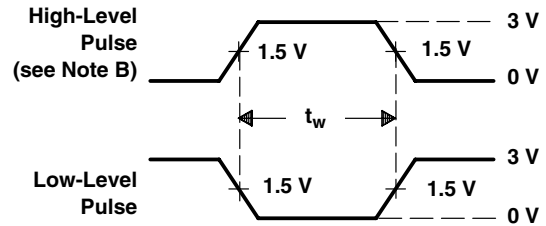
VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



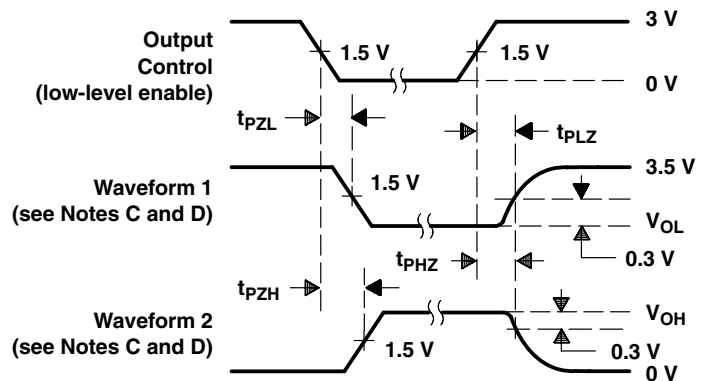
VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES (see Note D)



LOAD CIRCUIT FOR  
TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2.5$  ns, duty cycle = 50%.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. The outputs are measured one at a time with one transition per measurement.  
E. When measuring propagation delay times of 3-state outputs, switch S1 is open.  
F. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                  | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|------------------------------------------|-------------------------|
| 5962-9583501Q2A  | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9583501Q2A<br>SNJ54BCT<br>573FK | <a href="#">Samples</a> |
| 5962-9583501QRA  | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9583501QR<br>A<br>SNJ54BCT573J      | <a href="#">Samples</a> |
| 5962-9583501QSA  | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9583501QS<br>A<br>SNJ54BCT573W      | <a href="#">Samples</a> |
| SN74BCT573DW     | ACTIVE        | SOIC         | DW                 | 20   | 25             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | BCT573                                   | <a href="#">Samples</a> |
| SN74BCT573DWR    | ACTIVE        | SOIC         | DW                 | 20   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | BCT573                                   | <a href="#">Samples</a> |
| SN74BCT573N      | ACTIVE        | PDIP         | N                  | 20   | 20             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | SN74BCT573N                              | <a href="#">Samples</a> |
| SNJ54BCT573FK    | ACTIVE        | LCCC         | FK                 | 20   | 1              | TBD                        | POST-PLATE              | N / A for Pkg Type   | -55 to 125   | 5962-<br>9583501Q2A<br>SNJ54BCT<br>573FK | <a href="#">Samples</a> |
| SNJ54BCT573J     | ACTIVE        | CDIP         | J                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9583501QR<br>A<br>SNJ54BCT573J      | <a href="#">Samples</a> |
| SNJ54BCT573W     | ACTIVE        | CFP          | W                  | 20   | 1              | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9583501QS<br>A<br>SNJ54BCT573W      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54BCT573, SN74BCT573 :**

• Catalog: [SN74BCT573](#)

• Military: [SN54BCT573](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |                                                           |
|----|-----------------------------------------------------------|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74BCT573DWR | SOIC         | DW              | 20   | 2000 | 330.0              | 24.4               | 10.8    | 13.0    | 2.7     | 12.0    | 24.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74BCT573DWR | SOIC         | DW              | 20   | 2000 | 367.0       | 367.0      | 45.0        |

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



| PINS **<br>DIM | 14                     | 16                     | 18                     | 20                     |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A              | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC | 0.300<br>(7,62)<br>BSC |
| B MAX          | 0.785<br>(19,94)       | .840<br>(21,34)        | 0.960<br>(24,38)       | 1.060<br>(26,92)       |
| B MIN          | —                      | —                      | —                      | —                      |
| C MAX          | 0.300<br>(7,62)        | 0.300<br>(7,62)        | 0.310<br>(7,87)        | 0.300<br>(7,62)        |
| C MIN          | 0.245<br>(6,22)        | 0.245<br>(6,22)        | 0.220<br>(5,59)        | 0.245<br>(6,22)        |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



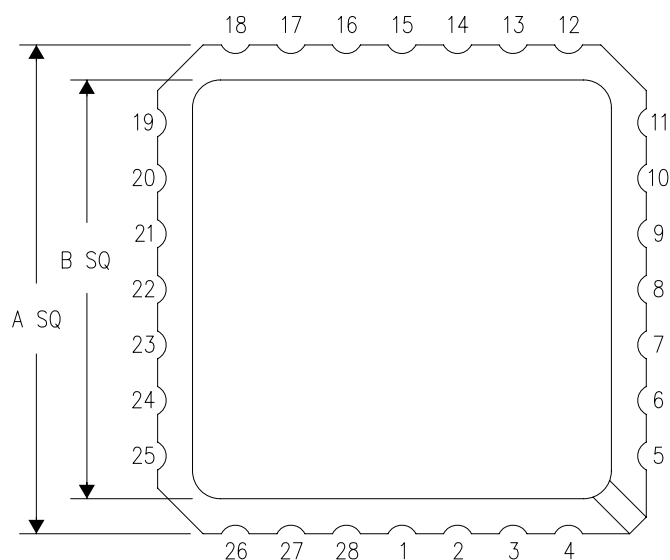
## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF<br>TERMINALS<br>** | A                |                  | B                |                  |
|---------------------------|------------------|------------------|------------------|------------------|
|                           | MIN              | MAX              | MIN              | MAX              |
| 20                        | 0.342<br>(8,69)  | 0.358<br>(9,09)  | 0.307<br>(7,80)  | 0.358<br>(9,09)  |
| 28                        | 0.442<br>(11,23) | 0.458<br>(11,63) | 0.406<br>(10,31) | 0.458<br>(11,63) |
| 44                        | 0.640<br>(16,26) | 0.660<br>(16,76) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 52                        | 0.740<br>(18,78) | 0.761<br>(19,32) | 0.495<br>(12,58) | 0.560<br>(14,22) |
| 68                        | 0.938<br>(23,83) | 0.962<br>(24,43) | 0.850<br>(21,6)  | 0.858<br>(21,8)  |
| 84                        | 1.141<br>(28,99) | 1.165<br>(29,59) | 1.047<br>(26,6)  | 1.063<br>(27,0)  |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



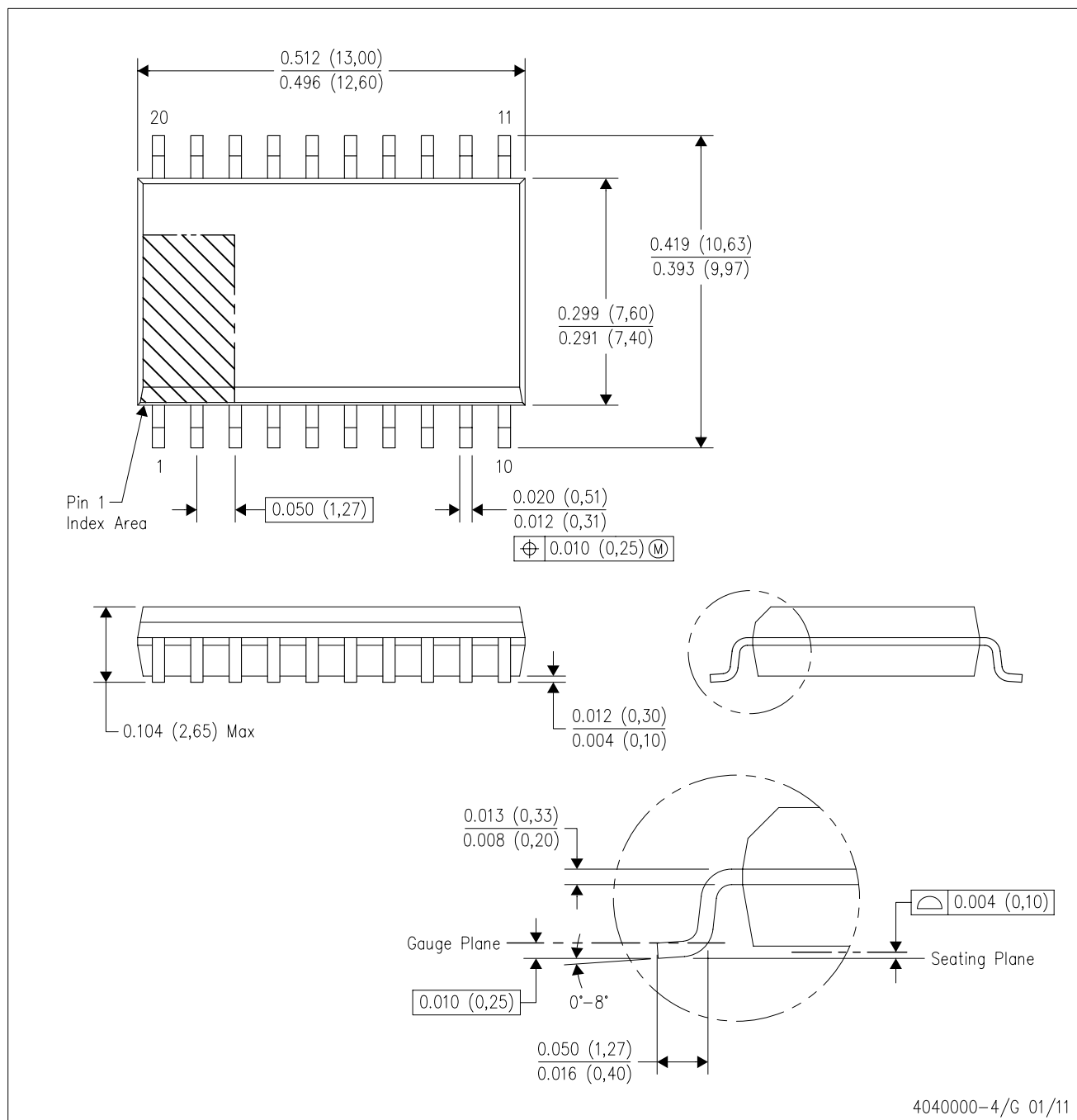
14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

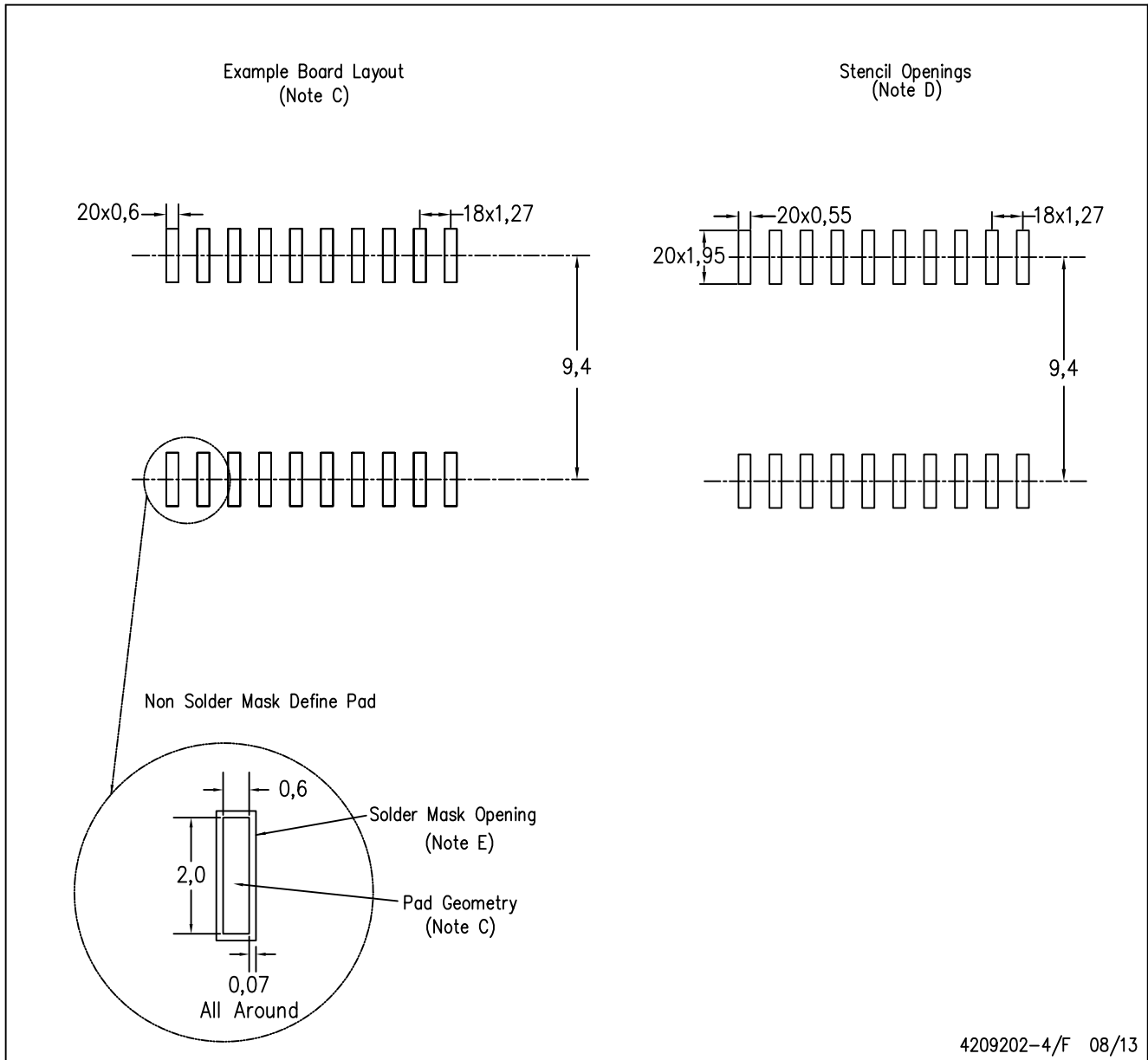
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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### Applications

|                               |                                                                                          |
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| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
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