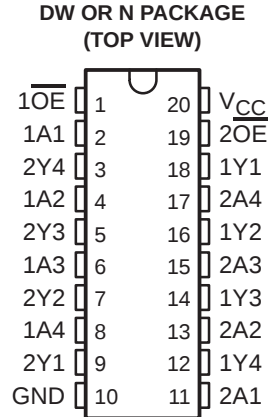


- BiCMOS Design Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- Package Options Include Plastic Small-Outline Packages (DW) and Standard Plastic 300-mil DIPs (N)

description

This octal buffer and line driver is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The SN74BCT756, SN74BCT757, and SN74BCT760 provide the choice of selected combinations of inverting outputs, symmetrical output-enable ($\overline{OE}$) inputs, and complementary OE and $\overline{OE}$ inputs.

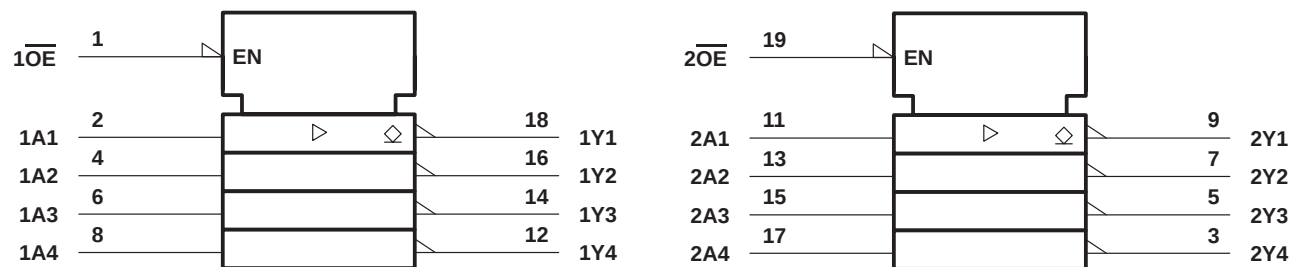
The SN74BCT756 is characterized for operation from 0°C to 70°C.



FUNCTION TABLE

INPUTS		OUTPUT
$\overline{OE}$	A	Y
H	X	H
L	L	H
L	H	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

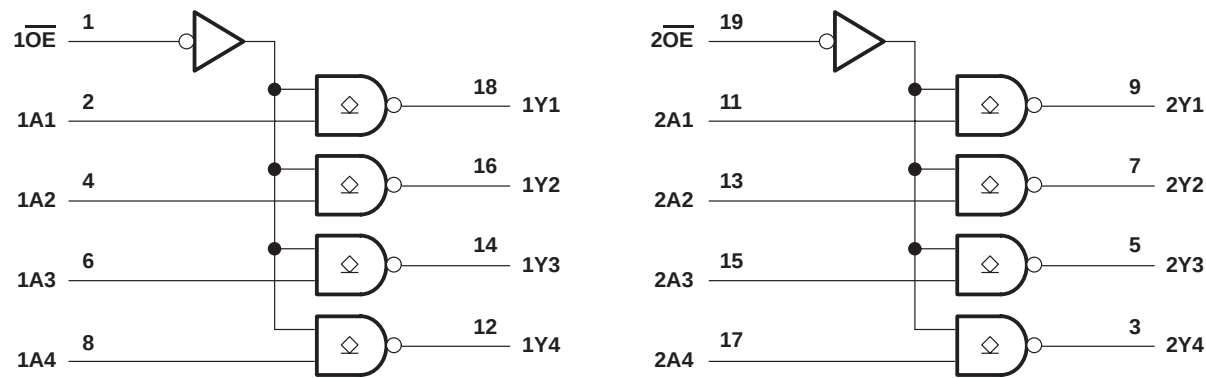


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I	–0.5 V to 7 V
Input current range, I_I	–30 mA to 5 mA
Voltage range applied to any output in the disabled or power-off state, V_O	–0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O	–0.5 V to V_{CC}
Current into any output in the low state	128 mA
Package thermal impedance, θ_{JA} (see Note 1): DW package	97°C/W
N package	67°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.5	5	5.5	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_{OH} High-level output voltage			5.5	V
I_{IK} Input clamp current			–18	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}	$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$			-1.2	V
I_{OH}	$V_{CC} = 4.5\text{ V}$,	$V_{OH} = 5.5\text{ V}$			0.1	mA
V_{OL}	$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 64\text{ mA}$		0.42	0.55	V
I_I	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$			0.1	mA
I_{IH}	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
I_{IL}	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.5\text{ V}$			-1	mA
I_{CC}	$V_{CC} = 5.5\text{ V}$,	Outputs open	Outputs high	21	33	mA
			Outputs low	55	86	
			$\overline{OE}$ disable	6	10	
C_i	$V_{CC} = 5\text{ V}$,	$V_I = 2.5\text{ V}$ or 0.5 V		6		pF
C_o	$V_{CC} = 5\text{ V}$,	$V_I = 2.5\text{ V}$ or 0.5 V		10		pF

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 1)

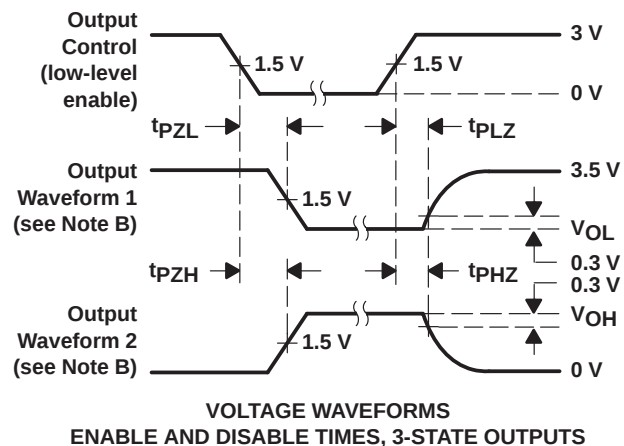
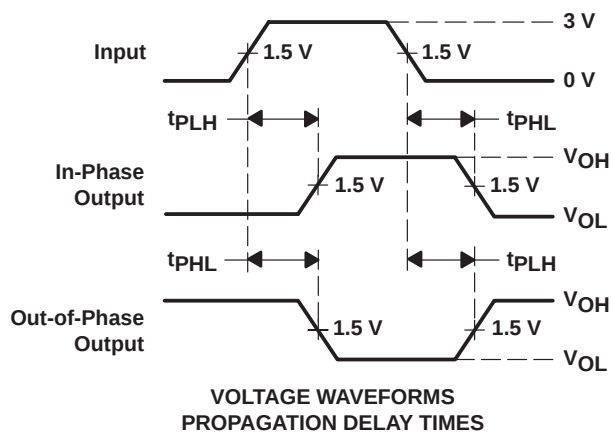
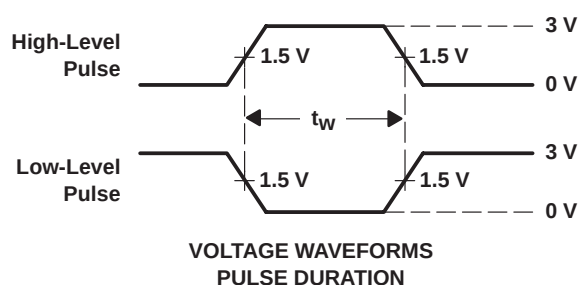
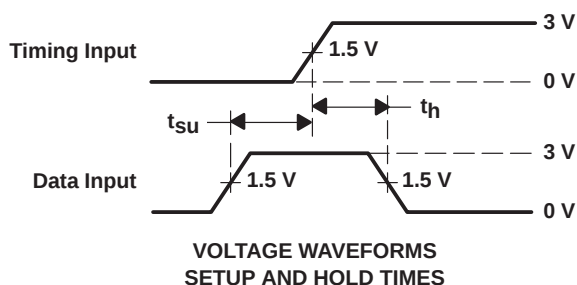
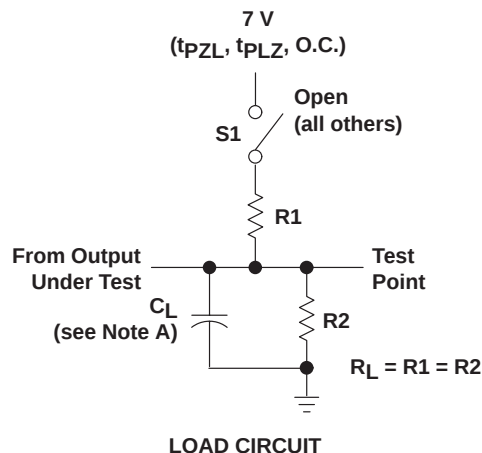
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = 25^\circ\text{C}$			$V_{CC} = 4.5\text{ to }5.5\text{ V}$, $C_L = 50\text{ pF}$, $R_1 = 500\ \Omega$, $R_2 = 500\ \Omega$, $T_A = \text{MIN to MAX}^\ddagger$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	6.2	8.5	10.5	6.2	11.3	ns
t_{PHL}			0.5	2	4.1	0.5	4.2	
t_{PLH}	$\overline{OE}$	Y	8.2	12.5	14.8	8.2	16.5	ns
t_{PHL}			3.4	6.8	9.2	3.4	10.3	

[‡] For conditions as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $t_r = t_f \leq 2.5 \text{ ns}$, duty cycle = 50%.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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