

# SN54LV273, SN74LV273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS195B – FEBRUARY 1993 – REVISED APRIL 1996

- **EPIC™ (Enhanced-Performance Implanted CMOS) 2-μ Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC}$ ,  $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model ( $C = 200$  pF,  $R = 0$ )**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), Ceramic Flat (W) Packages, Chip Carriers (FK), and (J) 300-mil DIPs**

## description

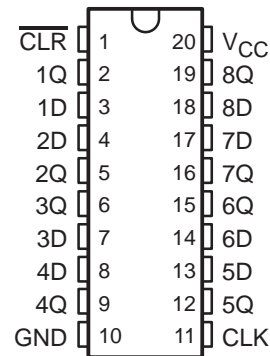
These octal D-type flip-flops are designed for 2.7-V to 5.5-V  $V_{CC}$  operation.

The 'LV273 are positive-edge-triggered flip-flops with direct clear ( $\overline{\text{CLR}}$ ) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

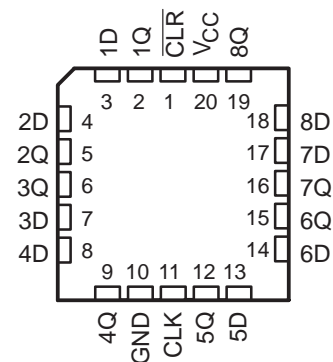
The SN74LV273 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LV273 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74LV273 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54LV273 . . . J OR W PACKAGE  
SN74LV273 . . . DB, DW, OR PW PACKAGE  
(TOP VIEW)



SN54LV273 . . . FK PACKAGE  
(TOP VIEW)



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**TEXAS  
INSTRUMENTS**

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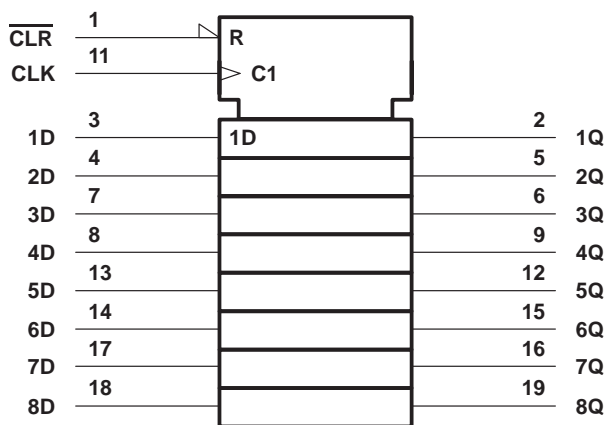
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FUNCTION TABLE  
(each flip-flop)

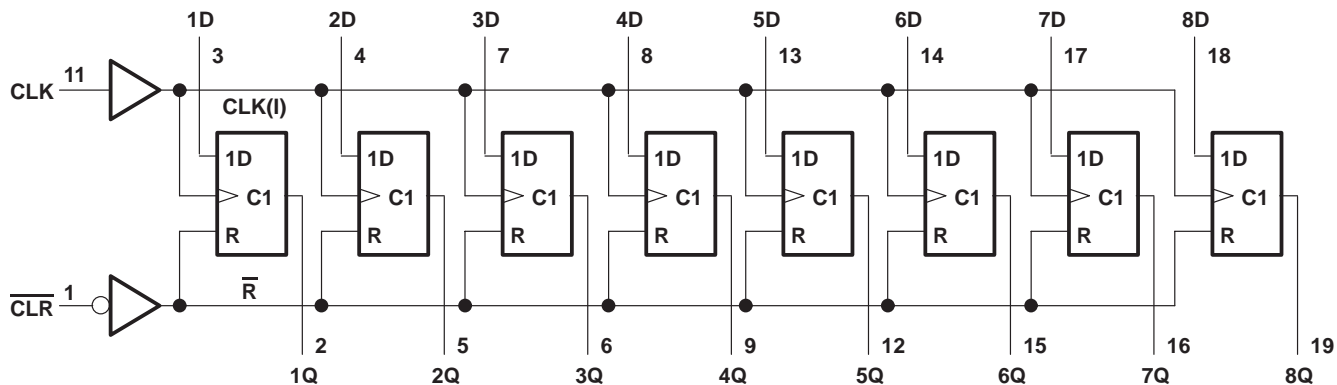
INPUTS			OUTPUT
CLR	CLK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DB, DW, J, PW, and W packages.

## logic diagram (positive logic)



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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±25 mA
Continuous current through $V_{CC}$ or GND .....	±50 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): DB package .....	0.6 W
DW package .....	1.6 W
PW package .....	0.7 W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. This value is limited to 7 V maximum.  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## recommended operating conditions (see Note 4)

		SN54LV273		SN74LV273		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	5.5	2.7	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2		V
		$V_{CC} = 4.5$ V to 5.5 V		3.15		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8		V
		$V_{CC} = 4.5$ V to 5.5 V		1.65		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V to 3.6 V		–6		mA
		$V_{CC} = 4.5$ V to 5.5 V		–12		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V to 3.6 V		6		mA
		$V_{CC} = 4.5$ V to 5.5 V		12		
$\Delta t/\Delta v$	Input transition rise or fall rate	0	100	0	100	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> †	SN54LV273			SN74LV273			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	MIN to MAX	V <sub>CC</sub> -0.2			V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -6 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = -12 mA	4.5 V	3.6			3.6			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	MIN to MAX	0.2			0.2			V
	I <sub>OL</sub> = 6 mA	3 V	0.4			0.4			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	±1			±1			μA
		5.5 V	±1			±1			
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	±5			±5			μA
		5.5 V	±5			±5			
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V	20			20			μA
		5.5 V	20			20			
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 3.6 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	2.5			2.5			pF
		5 V	3			3			

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN54LV273						UNIT
		V <sub>CC</sub> = 5.5 V ± 0.5 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	60	0	50	0	40	MHz
t <sub>w</sub>	Pulse duration	CLR low	6	10	12			ns
		CLK high or low	7	10	12			
t <sub>su</sub>	Setup time before CLK↑	Data	8	12	14			ns
		CLR inactive	2	2	2			
t <sub>h</sub>	Hold time, data after CLK↑	3	2	2			ns	

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		SN74LV273						UNIT
		V <sub>CC</sub> = 5.5 V ± 0.5 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	0	60	0	50	0	40	MHz
t <sub>w</sub>	Pulse duration	CLR low	6	10	12			ns
		CLK high or low	7	10	12			
t <sub>su</sub>	Setup time before CLK↑	Data	8	12	14			ns
		CLR inactive	2	2	2			
t <sub>h</sub>	Hold time, data after CLK↑	3	2	2			ns	

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LV273						UNIT		
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$				$V_{CC} = 2.7 \text{ V}$	
			MIN	TYP	MAX	MIN	TYP	MAX		MIN	MAX
$f_{\text{max}}$			60	100		50	80		40	MHz	
$t_{\text{pd}}$	CLK	Q		11	16		16	22		26	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q		13	22		14	24		30	ns

switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LV273						UNIT		
			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$				$V_{CC} = 2.7 \text{ V}$	
			MIN	TYP	MAX	MIN	TYP	MAX		MIN	MAX
$f_{\text{max}}$			60	100		50	80		40	MHz	
$t_{\text{pd}}$	CLK	Q		11	16		16	22		26	ns
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q		13	22		14	24		30	ns

operating characteristics,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance per flip-flop	$C_L = 50 \text{ pF}, f = 10 \text{ MHz}$	3.3 V	32	pF
			5 V	41	

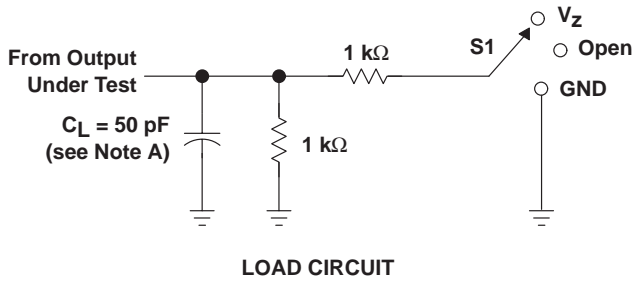
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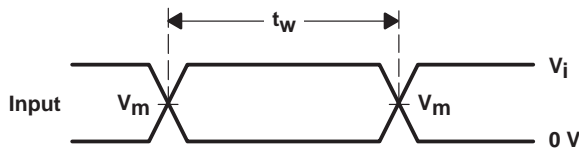
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## PARAMETER MEASUREMENT INFORMATION

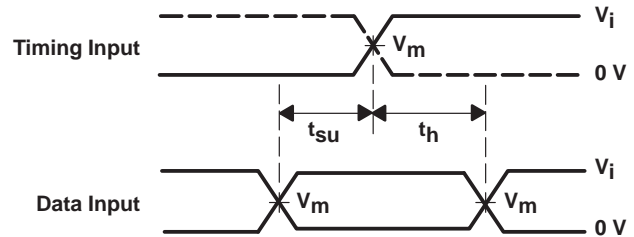


TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	V <sub>Z</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

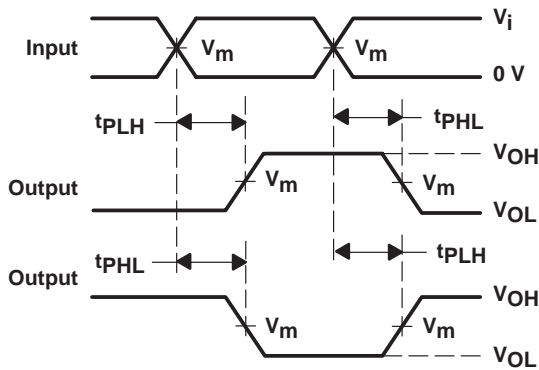
WAVEFORM CONDITION	V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> = 2.7 V to 3.6 V
V <sub>m</sub>	0.5 × V <sub>CC</sub>	1.5 V
V <sub>i</sub>	V <sub>CC</sub>	2.7 V
V <sub>Z</sub>	2 × V <sub>CC</sub>	6 V



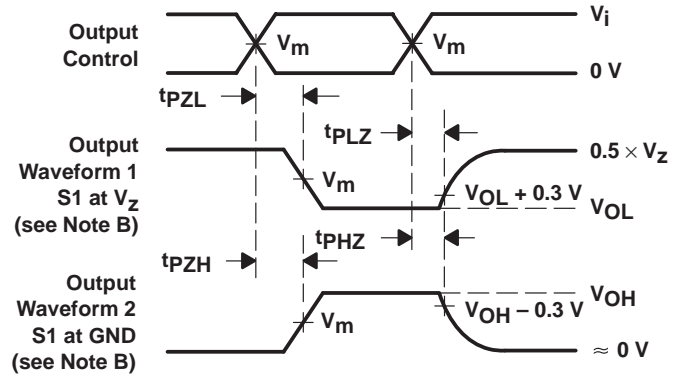
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C<sub>L</sub> includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.
  - The outputs are measured one at a time with one transition per measurement.
  - t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.
  - t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.
  - t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LV273DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74LV273DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LV273DWR	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
SN74LV273PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
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