

SN74LVC125A Quadruple Bus Buffer Gate With 3-State Outputs

1 Features

- 3-State outputs
- Separate \overline{OE} for all 4 buffers
- Operates from 1.65V to 3.6V
- Specified from -40°C to 85°C and -40°C to 125°C
- Inputs accept voltages to 5.5V
- Max t_{pd} of 4.8ns at 3.3V
- Typical V_{OLP} (output ground bounce) $< 0.8\text{V}$ at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) $> 2\text{V}$ at $V_{CC} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- Cable modem termination systems
- IP phones: wired and wireless
- Optical modules
- Optical networking:
 - EPON or video over fiber
- Point-to-point microwave backhaul
- Power: telecom DC/DC modules:
 - Analog or digital
- Private branch exchanges (PBX)
- TETRA base stations
- Telecom base band units
- Telecom shelters:
 - Filter units
 - Power distribution units (PDU)
 - Power monitoring units (PMU)
 - Wireless battery monitoring
 - Remote electrical tilt units (RET)
 - Remote radio units (RRU)
 - Tower mounted amplifiers (TMA)
- Vector signal analyzers and generators
- Video conferencing: IP-based HD
- WiMAX and wireless infrastructure equipment
- Wireless communications testers
- xDSL modems and DSLAM

3 Description

This quadruple bus buffer gate is designed for 1.65V to 3.6V V_{CC} operation.

The SN74LVC125A device features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V system environment.

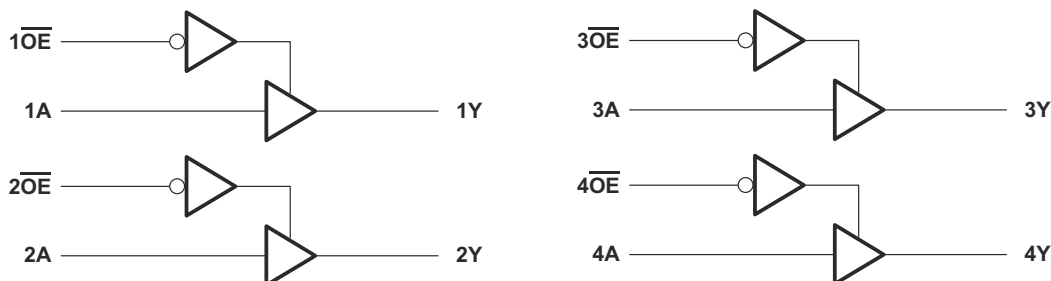
Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE ⁽³⁾
SN74LVC125A	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	D (SOIC, 14)	8.6 mm × 6mm	8.65mm × 3.91mm
	DB (SSOP, 14)	6.20mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 14)	10.2mm × 7.8mm	10.30mm × 5.30mm
	PW (TSSOP, 14)	5.00mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 14)	3.50mm × 3.50mm	3.50mm × 3.50mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.

(3) The body size (length × width) is a nominal value and does not include pins.



Simplified Schematic



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4 Pin Configuration and Functions

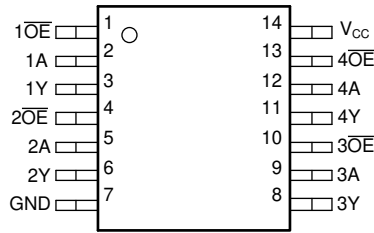


Figure 4-1. D, DB, NS, or PW Package (Top View)

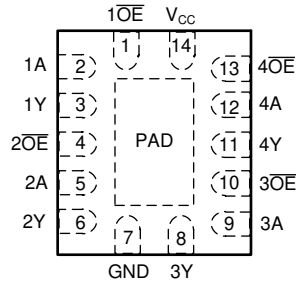


Figure 4-2. BQA or RGY Package (Top View)

Table 4-1. Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NAME	NO.		
1OE	1	Input	Output Enable
1A	2	Input	Input A
1Y	3	Output	Output Y
2OE	4	Input	Output Enable
2A	5	Input	Input A
2Y	6	Output	Output Y
GND	7	—	Ground
3Y	8	Output	Output Y
3A	9	Input	Input A
3OE	10	Input	Output Enable
4Y	11	Output	Output Y
4A	12	Input	Input A
4OE	13	Input	Output Enable
V _{CC}	14	—	Positive Supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Output voltage range ^{(2) (3)}	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-50 mA
I _{OK}	Output clamp current	V _O < 0		-50 mA
I _O	Continuous output current			±50 mA
	Continuous current through V _{CC} or GND			±100 mA
P _{tot}	Power dissipation	T _A = -40°C to 125°C ^{(4) (5)}		500 mW
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the [Section 5.3](#) table.
- (4) For the D package: above 70°C, the value of P_{tot} derates linearly with 8 mW/K.
- (5) For the DB, NS, and PW packages: above 60°C, the value of P_{tot} derates linearly with 5.5 mW/K.

5.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		$T_A = 25^\circ\text{C}$		$-40^\circ\text{C to } 85^\circ\text{C}$		$-40^\circ\text{C to } 125^\circ\text{C}$		UNIT	
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{CC}	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V_{IH}	High-level input voltage	$V_{CC} = 1.65\text{V to } 1.95\text{V}$	$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3\text{V to } 2.7\text{V}$	1.7		1.7		1.7		
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	2		2		2		
V_{IL}	Low-level input voltage	$V_{CC} = 1.65\text{V to } 1.95\text{V}$	$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3\text{V to } 2.7\text{V}$	0.7		0.7		0.7		
		$V_{CC} = 2.7\text{V to } 3.6\text{V}$	0.8		0.8		0.8		
V_I	Input voltage	0	5.5	0	5.5	0	5.5	V	
V_O	Output voltage	0	V_{CC}	0	V_{CC}	0	V_{CC}	V	
I_{OH}	High-level output current	$V_{CC} = 1.65\text{V}$	-4		-4		-4		mA
		$V_{CC} = 2.3\text{V}$	-8		-8		-8		
		$V_{CC} = 2.7\text{V}$	-12		-12		-12		
		$V_{CC} = 3\text{V}$	-24		-24		-24		
I_{OL}	Low-level output current	$V_{CC} = 1.65\text{V}$	4		4		4		mA
		$V_{CC} = 2.3\text{V}$	8		8		8		
		$V_{CC} = 2.7\text{V}$	12		12		12		
		$V_{CC} = 3\text{V}$	24		24		24		
$\Delta t/\Delta v$	Input transition rise or fall rate	8		8		8		ns/V	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾	SN74LVC125A						UNIT	
	BQA (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)		
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.3	127.8	140.4	123.8	150.8	92.1	$^\circ\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –100μA	1.65V to 3.6V	V _{CC} – 0.2			V _{CC} – 0.2		V _{CC} – 0.3		V
	I _{OH} = –4mA	1.65V	1.29			1.2		1.05		
	I _{OH} = –8mA	2.3V	1.9			1.7		1.55		
	I _{OH} = –12mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
I _{OH} = –24mA	3V	2.3			2.2		2			
V _{OL}	I _{OL} = 100μA	1.65V to 3.6V	0.1			0.2		0.3		V
	I _{OL} = 4mA	1.65V	0.24			0.45		0.6		
	I _{OL} = 8mA	2.3V	0.3			0.7		0.75		
	I _{OL} = 12mA	2.7V	0.4			0.4		0.6		
	I _{OL} = 24mA	3V	0.55			0.55		0.8		
I _I	V _I = 5.5V or GND	3.6V	±1			±5		±20		μA
I _{OZ}	V _O = V _{CC} or GND	3.6V	±1			±10		±20		μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	3.6V	1			10		40		μA
ΔI _{CC}	One input at V _{CC} – 0.6V, Other inputs at V _{CC} or GND	2.7V to 3.6V	500			500		5000		μA
C _i	V _I = V _{CC} or GND	3.3V	5							pF

5.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

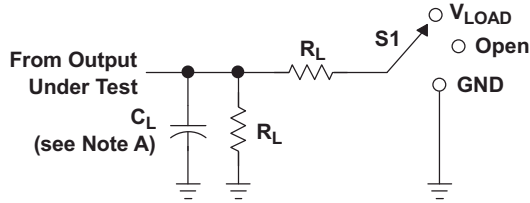
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	1.8V ± 0.15V	1	4.5	11.8	1	12.3	1	13.8	ns
			2.5V ± 0.2V	1	2.7	5.8	1	6.3	1	8.4	
			2.7V	1	3	5.3	1	5.5	1	7	
			3.3V ± 0.3V	1	2.5	4.6	1	4.8	1	6	
t _{en}	OE	Y	1.8V ± 0.15V	1	4.3	13.8	1	14.3	1	15.8	ns
			2.5V ± 0.2V	1	2.7	6.9	1	7.4	1	9.5	
			2.7V	1	3.3	6.4	1	6.6	1	8.5	
			3.3V ± 0.3V	1	2.4	5.2	1	5.4	1	7	
t _{dis}	OE	Y	1.8V ± 0.15V	1	4.3	10.6	1	11.1	1	12.6	ns
			2.5V ± 0.2V	1	2.2	5.1	1	5.6	1	7.7	
			2.7V	1	2.5	4.8	1	5	1	6.5	
			3.3V ± 0.3V	1	2.4	4.4	1	4.6	1	6	
t _{sk(o)}			3.3V ± 0.3V				1		1.5	ns	

5.7 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V _{CC}	TYP	UNIT
C _{pd}	Power dissipation capacitance per gate	f = 10MHz	1.8V	7.4	pF
			2.5V	11.3	
			3.3V	15	

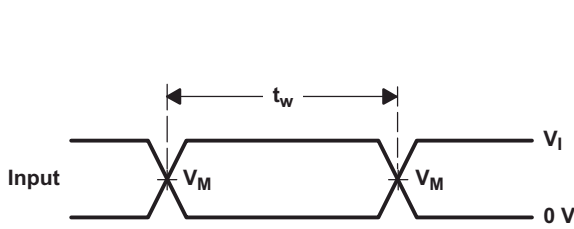
6 Parameter Measurement Information



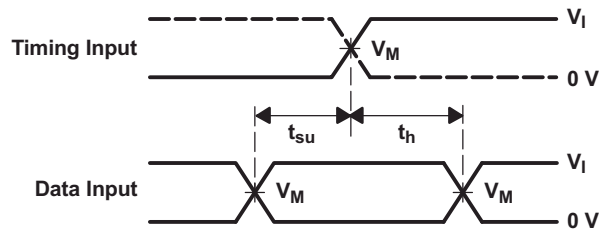
LOAD CIRCUIT

TEST	S1
t _{PLH} /t _{PHL}	Open
t _{PLZ} /t _{PZL}	V _{LOAD}
t _{PHZ} /t _{PZH}	GND

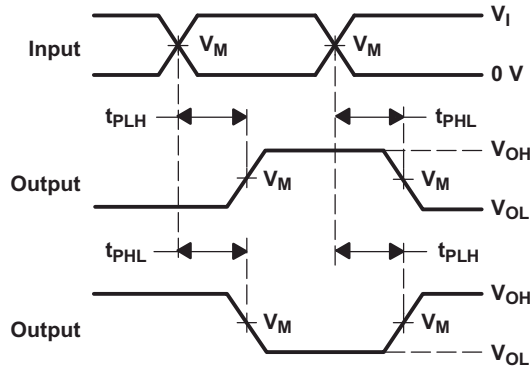
V _{CC}	INPUTS		V _M	V _{LOAD}	C _L	R _L	V _Δ
	V _I	t _r /t _f					
1.8 V ± 0.15 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V _{CC}	≤2 ns	V _{CC} /2	2 × V _{CC}	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



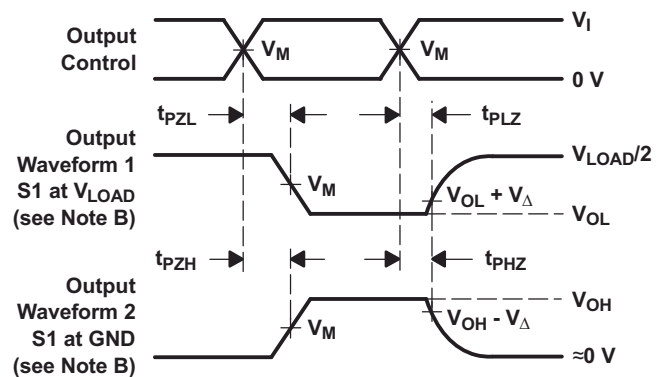
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - F. t_{PZL} and t_{PZH} are the same as t_{en}.
 - G. t_{PLH} and t_{PHL} are the same as t_{pd}.
 - H. All parameters and waveforms are not applicable to all devices.

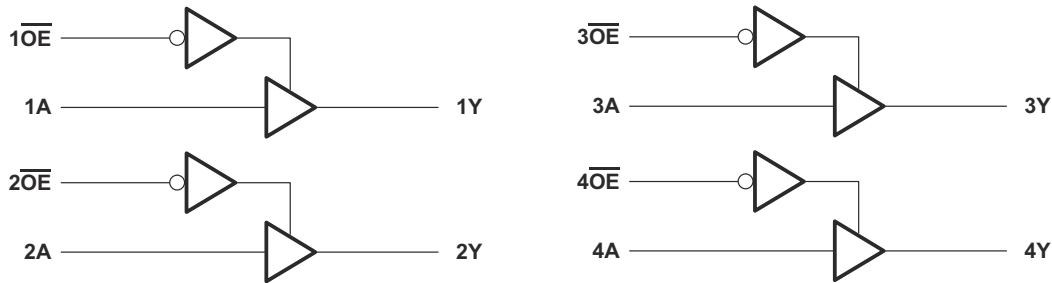
Figure 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74LVC125A device is a quadruple bus buffer gate featuring independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (\overline{OE}) input is high. When \overline{OE} is low, the respective gate passes the data from the A input to its Y output. To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65V to 5.5V
- Allows down voltage translation
- Inputs accept voltages to 5.5V

7.4 Device Functional Modes

Table 7-1. Function Table

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Typical Application

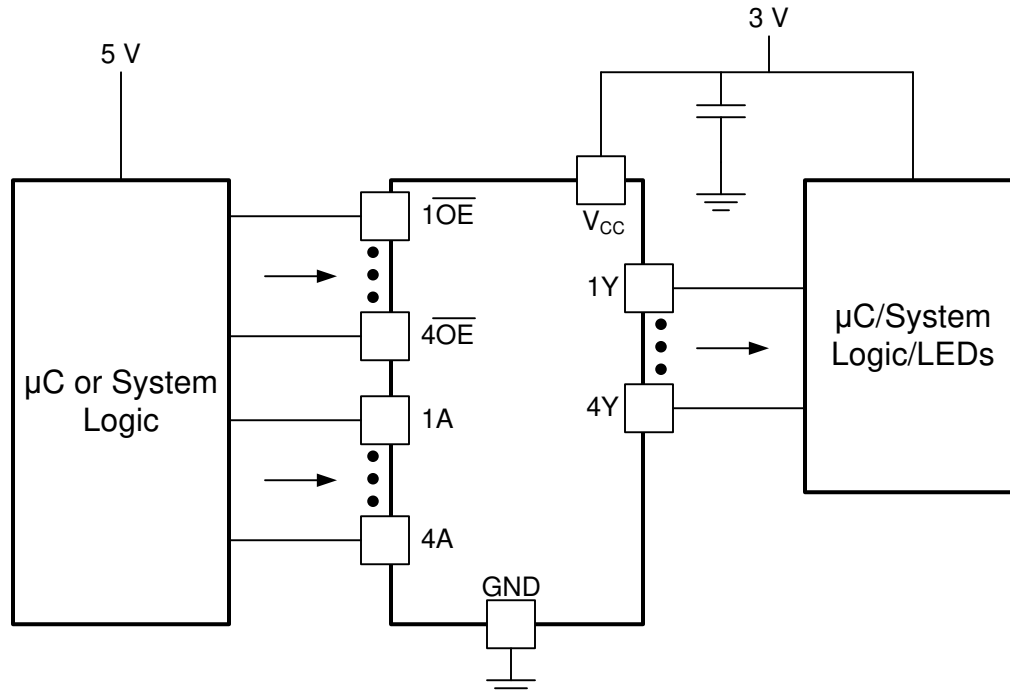


Figure 8-1. Typical Application Schematic

8.1.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

8.1.2 Detailed Design Procedure

1. Recommended Input Conditions:

- For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the [Section 5.3](#) table.
- For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [Section 5.3](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as $(V_I \text{ max})$ in the [Section 5.3](#) table at any valid V_{CC} .

2. Recommend Output Conditions:

- Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Section 5.1](#) table.
- Outputs should not be pulled above V_{CC} .
- Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

8.1.3 Application Curves

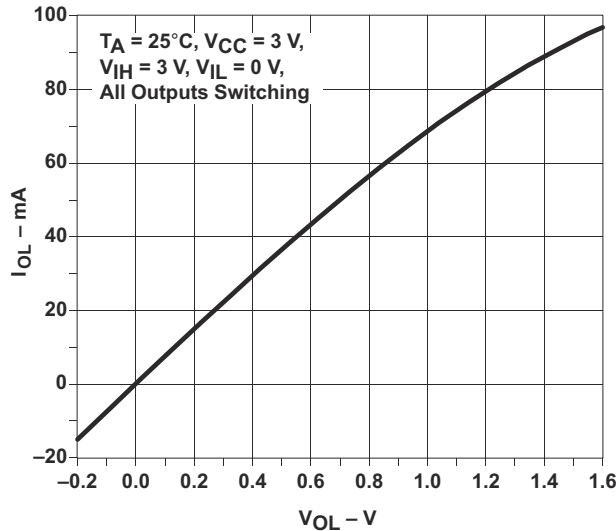


Figure 8-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

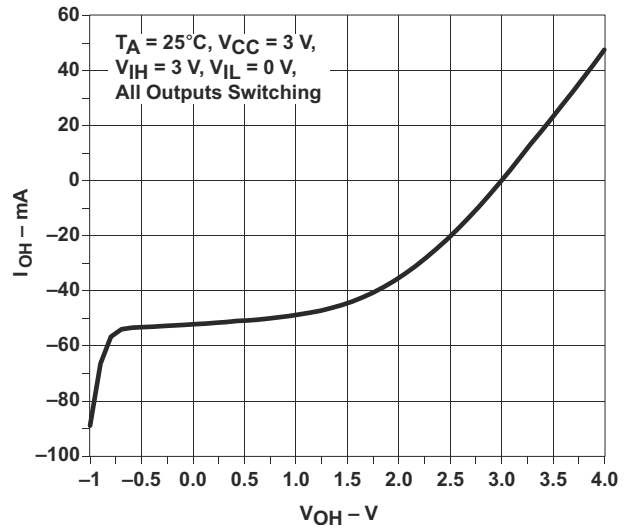


Figure 8-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

8.2 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 5.3](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μf is recommended; if there are multiple V_{CC} pins, then 0.01 μf or 0.022 μf is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μf and a 1 μf are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.3 Layout

8.3.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 8-4](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

8.3.2 Layout Example

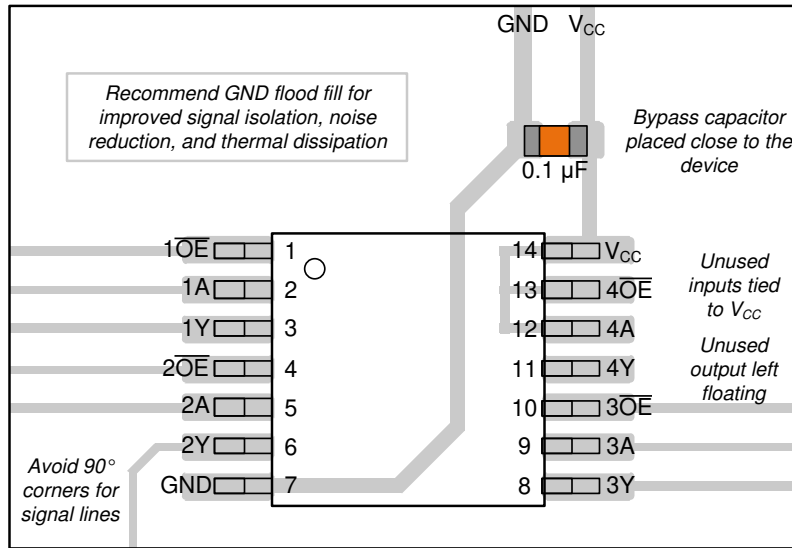


Figure 8-4. Example layout for the SN74LVC125A

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LVC125A	Click here	Click here	Click here	Click here	Click here

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

Changes from Revision S (May 2024) to Revision T (September 2024)	Page
• Updated thermal values for D package from RθJA = 86 to 127.8, all values in °C/W	5

Changes from Revision R (February 2024) to Revision S (May 2024)	Page
• Updated RθJA values: DB = 96 to 140.4, NS = 76 to 123.8, PW = 113 to 150.8, RGY = 47 to 92.1; Updated DB, NS, PW, and RGY packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W.....	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC125ABQAR	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LVC125ABQAR.A	Active	Production	WQFN (BQA) 14	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LV125A
SN74LVC125AD	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125AD.B	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADBR	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADBR.A	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADBR.B	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADBRG4	Active	Production	SSOP (DB) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ADE4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADG4	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADR	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADR.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADR.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRE4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG3	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG3.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG4	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADRG4.B	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADT	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADT.B	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ADTG4	Active	Production	SOIC (D) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANS.B	Active	Production	SOP (NS) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSR	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSR.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSR.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSRG4	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSRG4.A	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125ANSRG4.B	Active	Production	SOP (NS) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC125A
SN74LVC125APW	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74LVC125APW.B	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWE4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWG4	Active	Production	TSSOP (PW) 14	90 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWR.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRE4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG3	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LC125A
SN74LVC125APWRG3.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG3.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG4	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG4.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWRG4.B	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWT	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWT.B	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWTE4	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125APWTG4	Active	Production	TSSOP (PW) 14	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC125A
SN74LVC125ARGYR	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC125A
SN74LVC125ARGYR.A	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC125A
SN74LVC125ARGYR.B	Active	Production	VQFN (RGY) 14	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC125A

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC125A :

- Automotive : [SN74LVC125A-Q1](#)
- Enhanced Product : [SN74LVC125A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC125ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC125ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC125ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ADRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.3	8.0	16.0	Q1
SN74LVC125ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC125ANSR	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC125ANSRG4	SOP	NS	14	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWRG3	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1
SN74LVC125APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC125ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC125ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC125ADBR	SSOP	DB	14	2000	353.0	353.0	32.0
SN74LVC125ADR	SOIC	D	14	2500	353.0	353.0	32.0
SN74LVC125ADRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74LVC125ADRG4	SOIC	D	14	2500	333.2	345.9	28.6
SN74LVC125ADT	SOIC	D	14	250	213.0	191.0	35.0
SN74LVC125ANSR	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC125ANSRG4	SOP	NS	14	2000	353.0	353.0	32.0
SN74LVC125APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC125APWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125APWRG3	TSSOP	PW	14	2000	366.0	364.0	50.0
SN74LVC125APWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74LVC125APWT	TSSOP	PW	14	250	353.0	353.0	32.0
SN74LVC125ARGYR	VQFN	RGY	14	3000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVC125AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125AD.B	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125ADE4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC125ANS.B	NS	SOP	14	50	530	10.5	4000	4.1
SN74LVC125APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC125APW.B	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC125APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC125APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5

D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



EXAMPLE BOARD LAYOUT

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

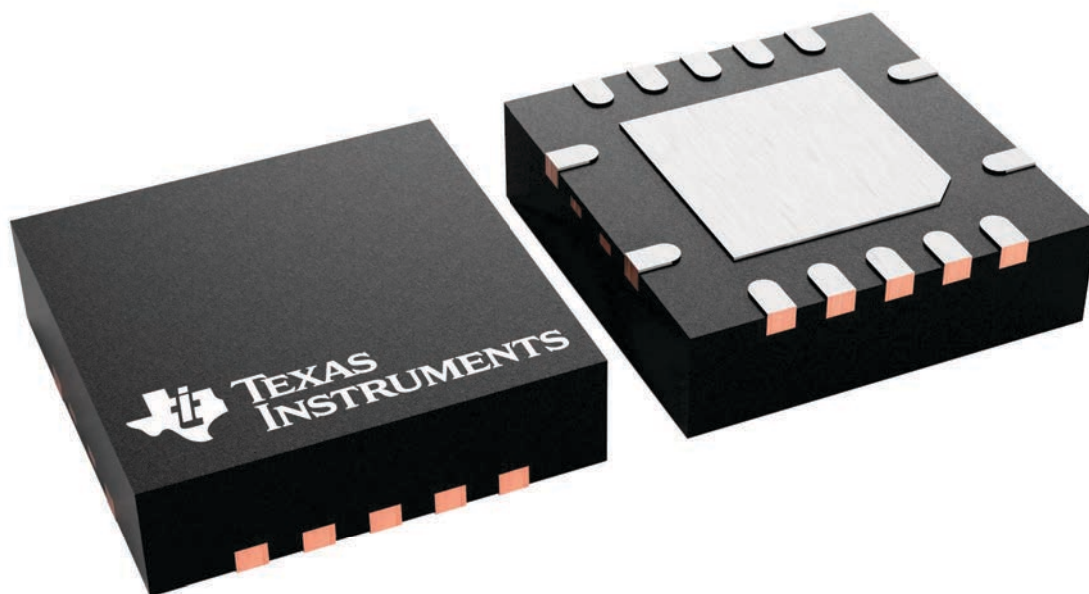
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

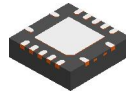
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

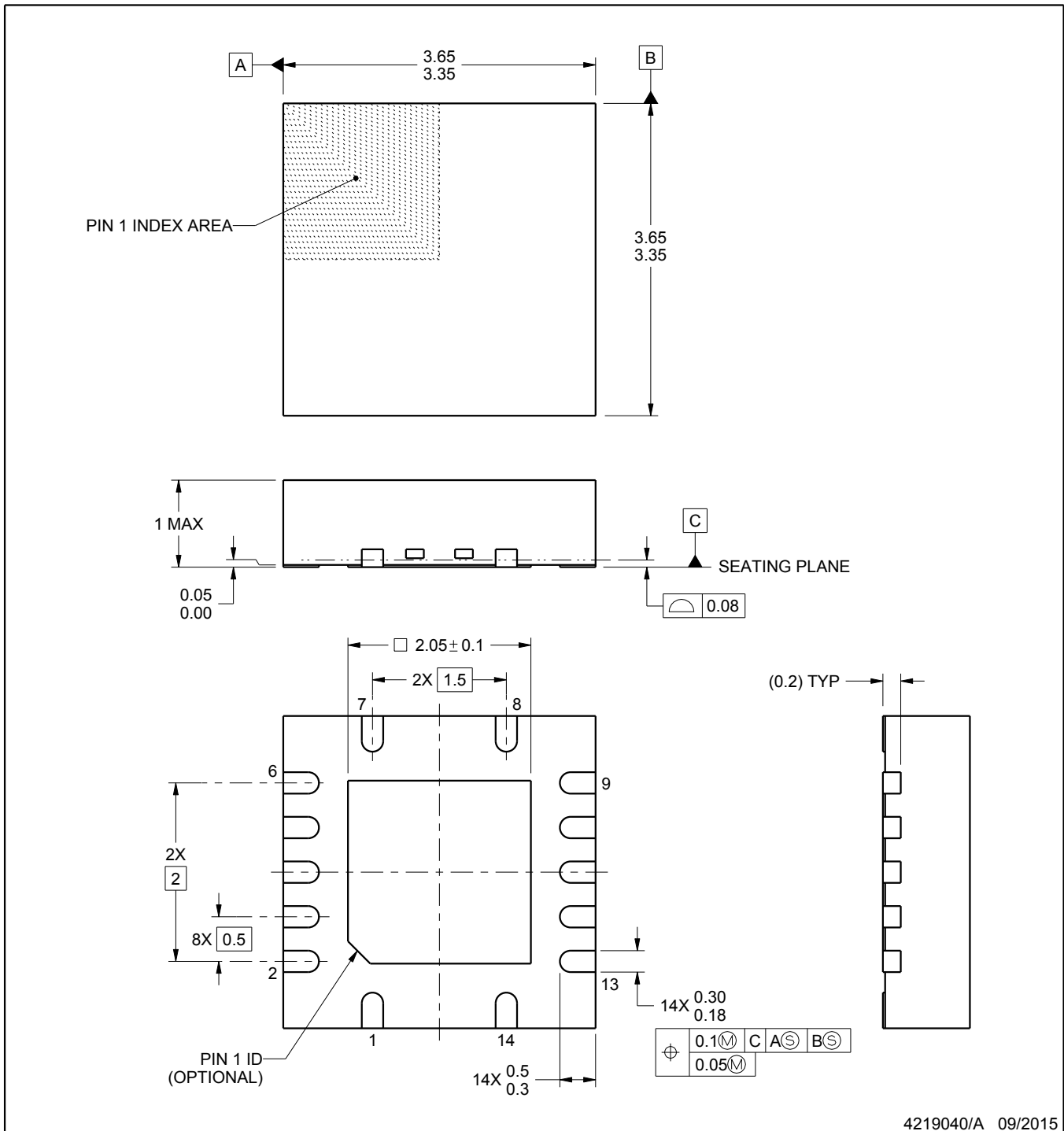
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

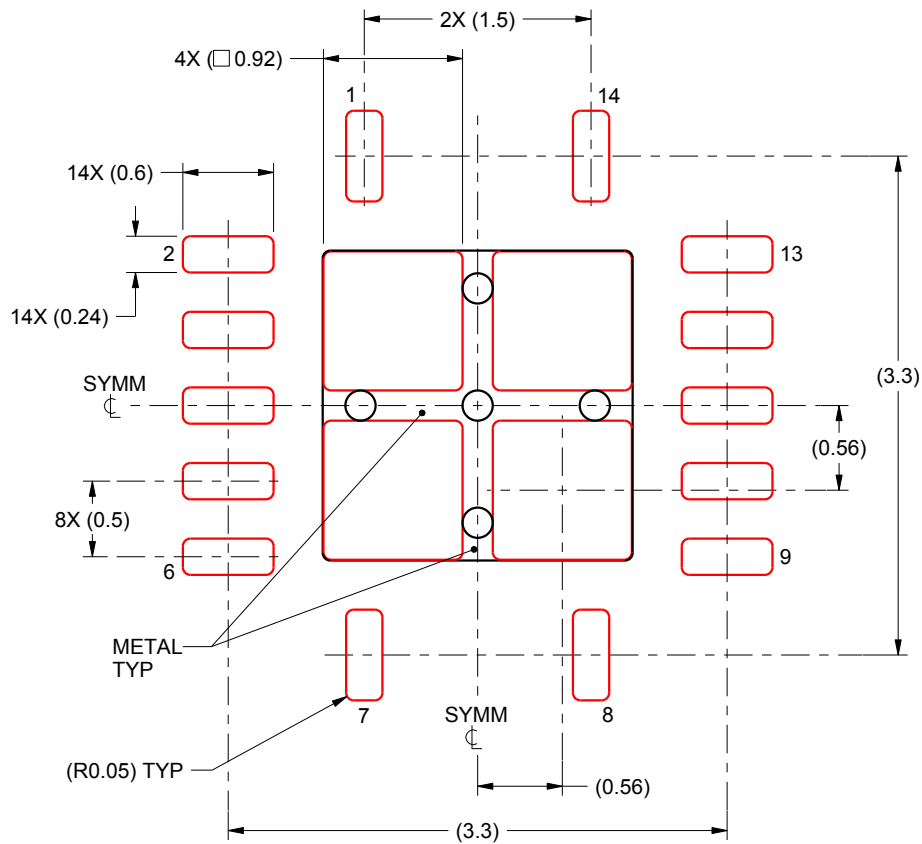
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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