2.7 V TO 5.5 V, 12- AND 10-BIT OCTAL DAC IN WAFER CHIP SCALE PACKAGE

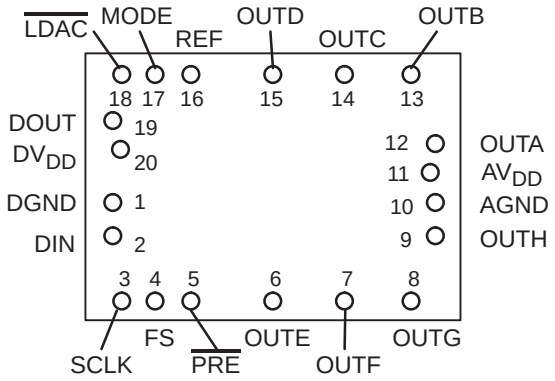
FEATURES

- **Eight Voltage Output DACs in One Package**
  - **TLV5610IYE . . . 12-Bit**
  - **TLV5608IYE . . . 10-Bit**
- **Programmable Settling Time vs Power Consumption**
  - **1 μs in Fast Mode**
  - **3 μs in Slow Mode**
- **Compatible With TMS320™ DSP Family and SPI Serial Ports**
- **Monotonic Over Temperature**
- **Low Power Consumption:**
  - **18 mW in Slow Mode at 3 V**
  - **48 mW in Fast Mode at 3 V**
- **Power Down Mode**
- **Buffered, High Impedance Reference Inputs**
- **Data Output for Daisy Chainin**

APPLICATIONS

- **Digital Servo Control Loops**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

WCS PACKAGE
(BOTTOM VIEW)



DESCRIPTION

The TLV5610IYE and TLV5608IYE are pin compatible eight channel 12-/10-bit voltage output DACs each with a flexible serial interface. The serial interface allows glueless interface to TMS320 and SPI, QSPI, and Microwire serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

Additional features are a power-down mode, an $\overline{\text{LDAC}}$ input for simultaneous update of all eight DAC outputs, and a data output which can be used to cascade multiple devices.

The resistor string output voltage is buffered by a rail-to-rail output amplifier with a programmable settling time to allow the designer to optimize speed vs power dissipation. The buffered, high-impedance reference input can be connected to the supply voltage.

The TLV5610IYE and TLV5608IYE implemented with a CMOS process and are available in a 20-terminal WCS package. The TLV5610IYE and TLV5608IYE are characterized for operation from −40°C to 85°C in a wire-bonded small outline (SOIC) package.

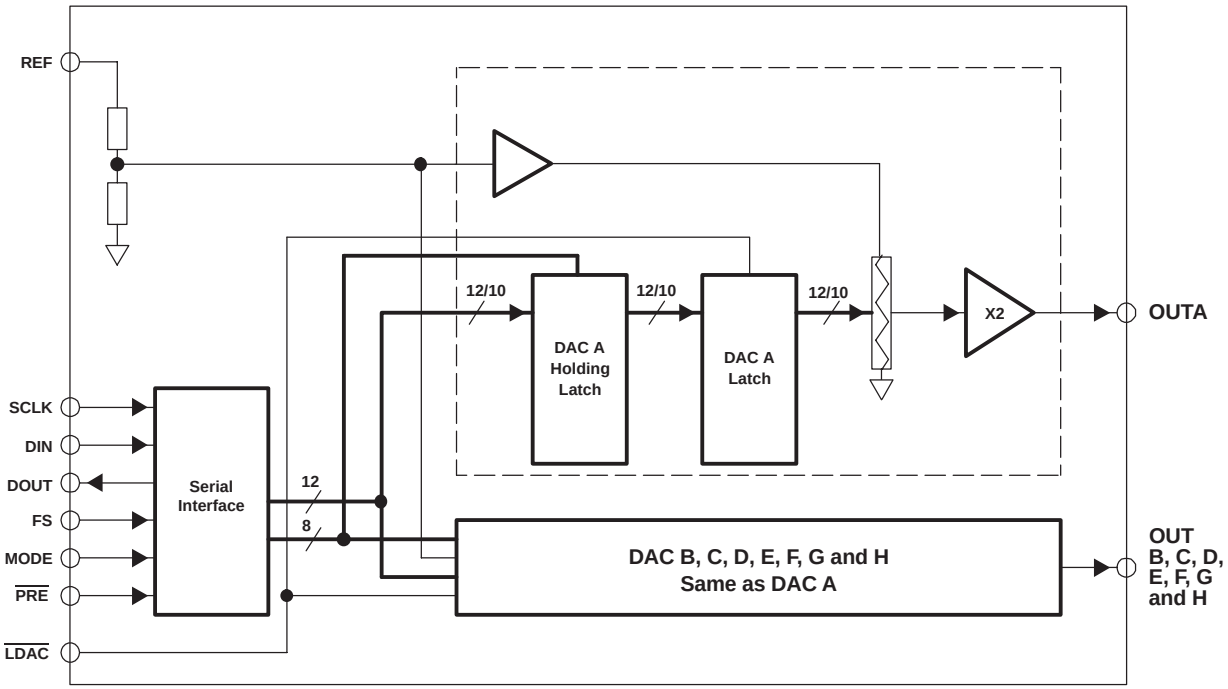
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGE
	WCS(1) (YE)
−40°C to 85°C	TLV5610IYE
	TLV5608IYE

(1) Wafer chip scale package. See Figure 13.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	10	P	Analog ground
AV_{DD}	11	P	Analog power supply
DGND	1	P	Digital ground
DIN	2	I	Digital serial data input
DOUT	19	O	Digital serial data output
DV_{DD}	20	P	Digital power supply
FS	4	I	Frame sync input
$\overline{\text{LDAC}}$	18	I	Load DAC. The DAC outputs are only updated, if this signal is low. It is an asynchronous input.
MODE	17	I	DSP/µC mode pin. High = µC mode, NC = DSP mode.
$\overline{\text{PRE}}$	5	I	Preset input
REF	16	I	Voltage reference input
SCLK	3	I	Serial clock input
OUTA−OUTH	12−15, 6−9	O	DAC outputs A, B, C, D, E, F, G and H

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage, (AV_{DD}, DV_{DD} to GND)	7 V
Reference input voltage range	− 0.3 V to AV_{DD} + 0.3
Digital input voltage rang	− 0.3 V to DV_{DD} + 0.3
Operating free-air temperature range, T_A	−40°C to 85°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
Supply voltage, AV_{DD}, AV_{DD}	5-V operation	4.5	5	5.5	V
	3-V operation	2.7	3	3.3	V
High level digital input, V_{IH}	DV_{DD} = 2.7 V to 5.5 V	2			V
Low level digital input, V_{IL}	DV_{DD} = 2.7 V to 5.5 V			0.8	V
Reference voltage, V_{ref}	AV_{DD} = 5 V	GND	4.096	AV_{DD}	V
	AV_{DD} = 3 V	GND	2.048	AV_{DD}	
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Clock frequency, f_{CLK}				30	MHz
Operating free-air temperature, T_A		−40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted(1)

POWER-SUPPLY								
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = DV_{DD} or GND	V_{ref} = 4.096 V,	Fast		16	21	mA
				Slow		6	8	
	Power-down supply current					0.1		µA
POR	Power on threshold					2		V
PSRR	Power supply rejection ratio	Full scale, See Note 1				−60		dB

STATIC DAC SPECIFICATIONS							
	Resolution	TLV5610IYE				12		Bits
		TLV5608IYE				10		
INL	Integral nonlinearity	TLV5610IYE	V_{ref} = 2 V, 4 V	Code 40 to 4095		±2	±6	LSB
		TLV5608IYE		Code 20 to 1023		±0.5	±2	
DNL	Differential nonlinearity	TLV5610IYE	V_{ref} = 2 V, 4 V	Code 40 to 4095		±0.5	±1	LSB
		TLV5608IYE		Code 20 to 1023		±0.1	±1	
E_{ZS}	Zero scale error (offset error at zero scale)						±30	mV
E_{ZS} TC	Zero scale error temperature coefficient					30		µV/°C
E_G	Gain error						±0.6	%Full Scale V
E_GTC	Gain error temperature coefficient					10		ppm/°C

(1) Power supply rejection ratio at full scale is measured by varying AV_{DD} and is given by:
PSRR = 20 log [($E_G(AV_{DD}max) – E_G(AV_{DD}min)$)/$V_{DD}max$]

ELECTRICAL CHARACTERISTICS (CONTINUED)

over operating free-air temperature range unless otherwise noted(1)

OUTPUT SPECIFICATIONS						
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ		0		AV_{DD}−0.4	V
	Output load regulation accuracy	R_L = 2 kΩ vs 10 kΩ				±0.3	%Full Scale V

REFERENCE INPUT							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_I	Input voltage range			0		AV_{DD}	V
R_I	Input resistance				100		kΩ
C_i	Input capacitance				5		pF
	Reference input bandwidth	V_{ref} = 0.4 V_{pp} + 2.048 Vdc, Input code = 0x800	Fast		2.2		MHz
			Slow		1.9		MHz
	Reference feedthrough	V_{ref} = 2 V_{pp} at 1 kHz + 2.048 Vdc (see Note 1)			−84		dB

(1) Reference feedthrough is measured at the DAC output with an input code = 0x000.

DIGITAL INPUTS						
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current		V_I = DV_{DD}			1	µA
I_{IL}	Low-level digital input current		V_I = 0 V	−1			µA
C_i	Input capacitance				8		pF

DIGITAL OUTPUTS						
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level digital output voltage	R_L = 10 kΩ		2.6			V
V_{OL}	Low-level digital output voltage	R_L = 10 kΩ				0.4	V
	Output voltage rise time	R_L = 10 kΩ, C_L = 20 pF, Includes propogation delay			7	20	ns

ANALOG OUTPUT DYNAMIC PERFORMANCE								
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ,	C_L = 100 pF, See Note 1	Fast		1	3	µs
				Slow		3	7	
$t_{s(CC)}$	Output settling time, code to code	R_L = 10 kΩ,	C_L = 100 pF, See Note 2	Fast		0.5	1	µs
				Slow		1	2	
SR	Slew rate	R_L = 10 kΩ,	C_L = 100 pF, See Note 3	Fast	4	10		V/µs
				Slow	1	3		
	Glitch energy	See Note 4				4		nV−s
	Channel crosstalk	10 kHz sine, 4 V_{PP}				−90		dB

(1) Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x80 to 0xFFF and 0xFFF to 0x080 respectively. Assured by design; not tested.

(2) Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full scale. Assured by design; not tested.

(3) Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full scale voltage.

(4) Code transition: TLV5610IYE − 0x7FF to 0x800, TLV5608IYE − 0x7FC to 0x800.

DIGITAL INPUT TIMING REQUIREMENTS

PARAMETER		MIN	TYP	MAX	UNIT
$t_{su(FS-CK)}$	Setup time, FS low before first negative SCLK edge	8			ns
$t_{su(C16-FS)}$	Setup time, 16th negative edge after FS low on which bit D0 is sampled before rising edge of FS. µC mode only	10			ns
$t_{wL(LDAC)}$	$\overline{\text{LDAC}}$ duration low	10			ns
t_{wH}	SCLK pulse duration high	16			ns
t_{wL}	SCLK pulse duration low	16			
$t_{su(D)}$	Setup time, data ready before SCLK falling edge	8			ns
$t_{h(D)}$	Hold time, data held valid after SCLK falling edge	5			ns
$t_{wH(FS)}$	FS duration high	10			ns
$t_{wL(FS)}$	FS duration low	10			ns
t_s	Settling time	See AC specs			

TYPICAL CHARACTERISTICS

OUTPUT LOAD REGULATION

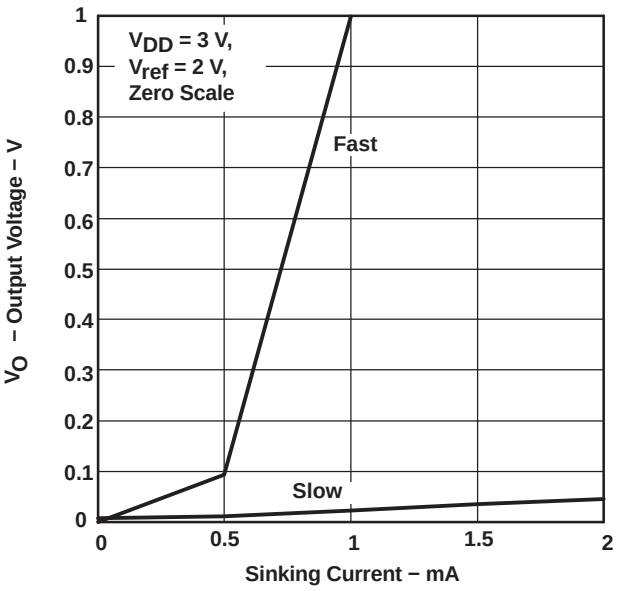


Figure 1

OUTPUT LOAD REGULATION

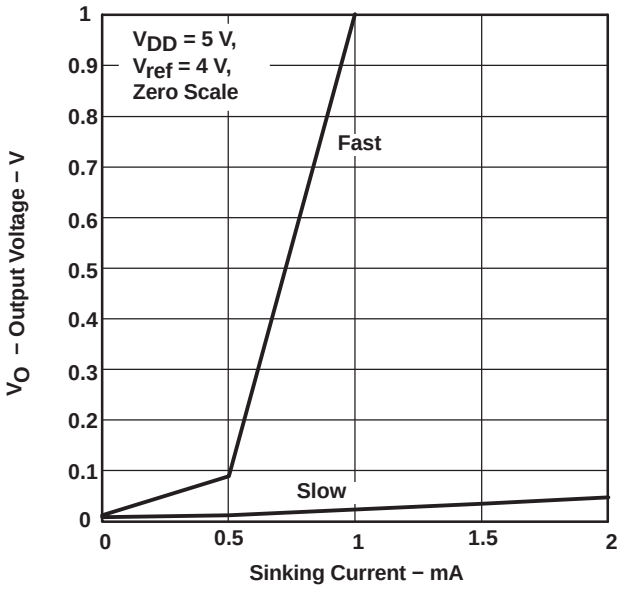


Figure 2

OUTPUT LOAD REGULATION

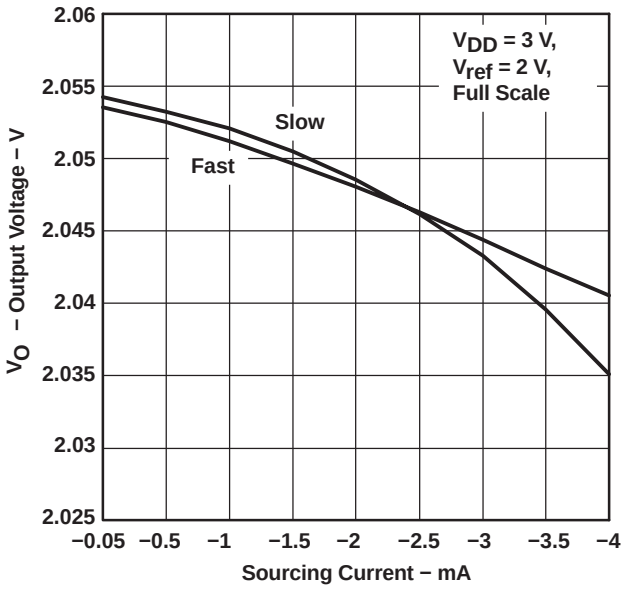


Figure 3

OUTPUT LOAD REGULATION

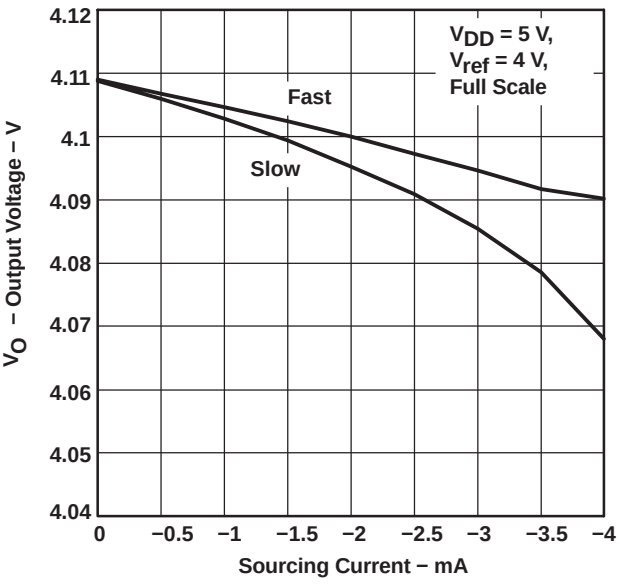


Figure 4

TLV5610IYE
INTEGRAL NONLINEARITY
vs
CODE

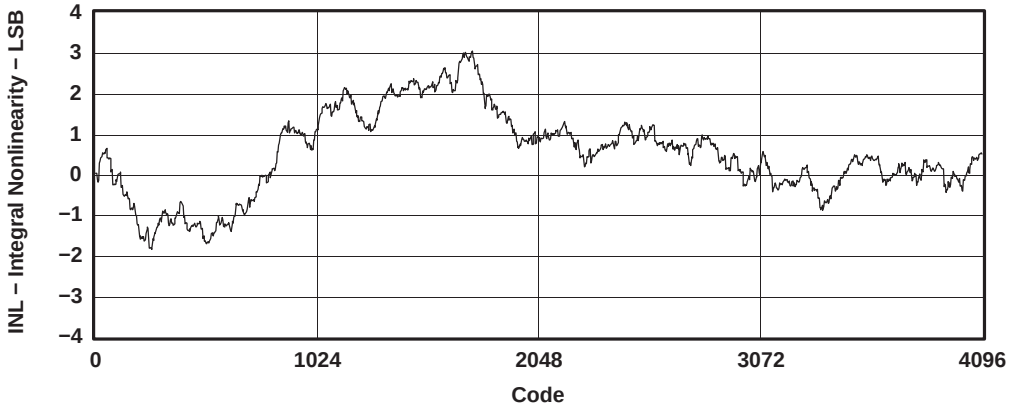


Figure 5

TLV5610IYE
DIFFERENTIAL NONLINEARITY
vs
CODE

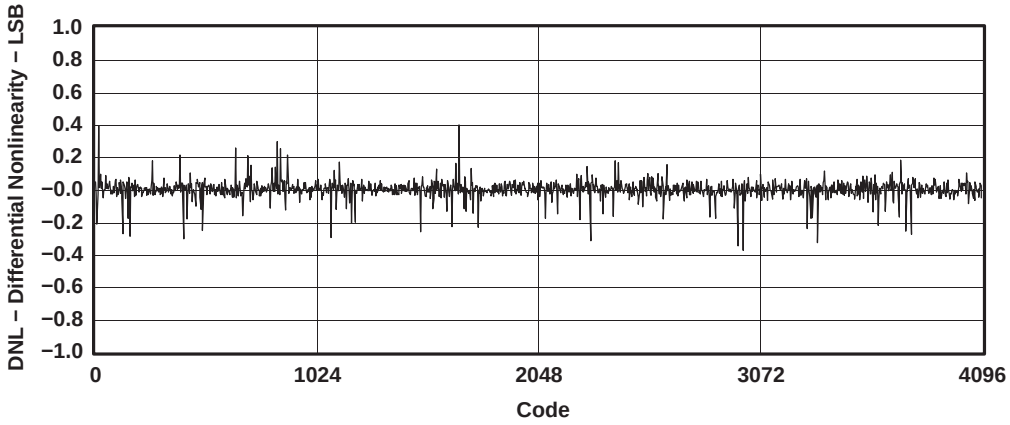


Figure 6

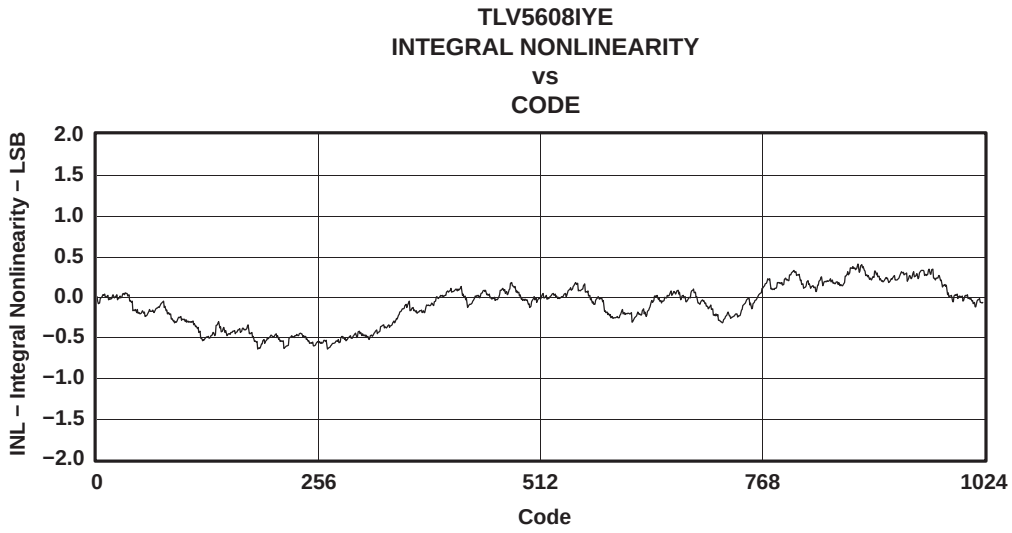


Figure 7

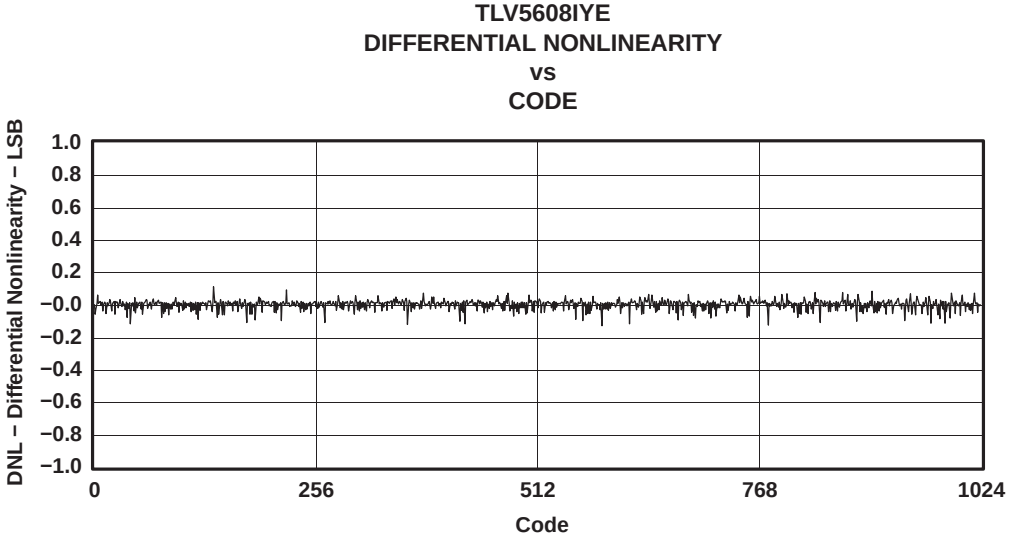
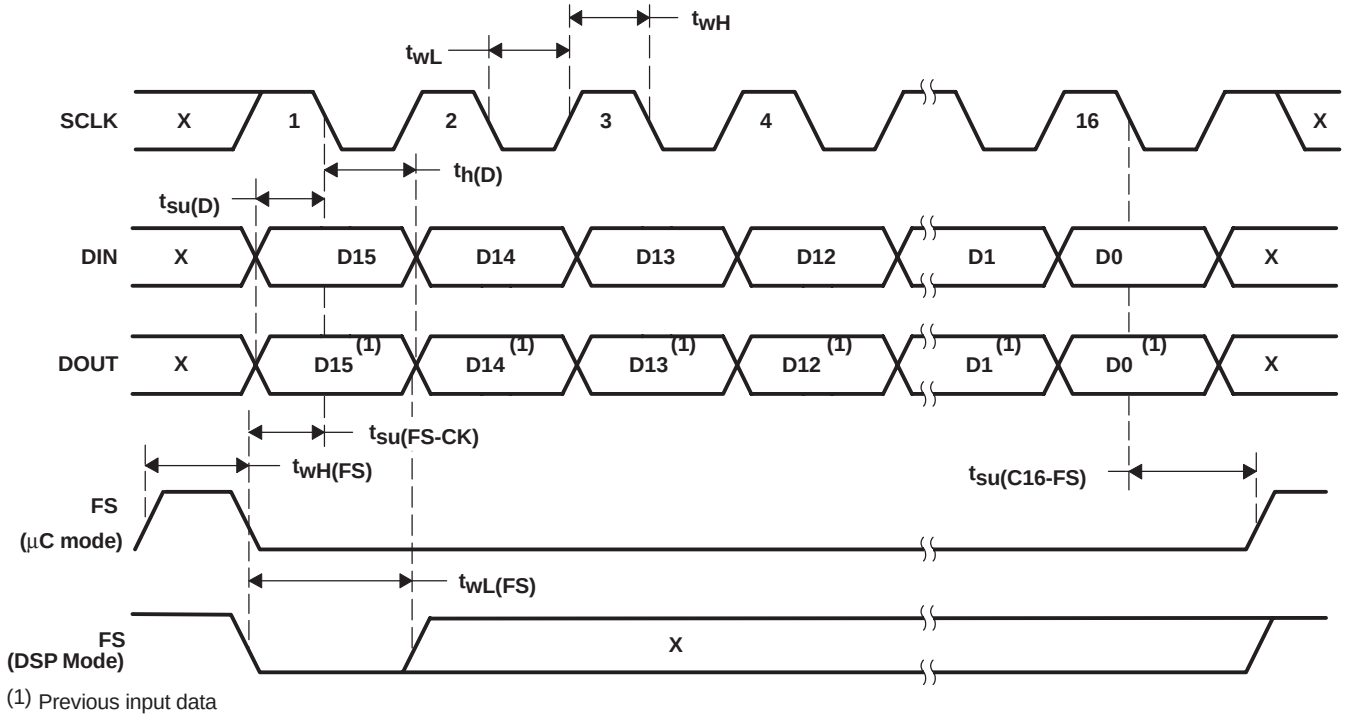


Figure 8

PARAMETER MEASUREMENT INFORMATION



(1) Previous input data

Figure 9. Serial Interface Timing

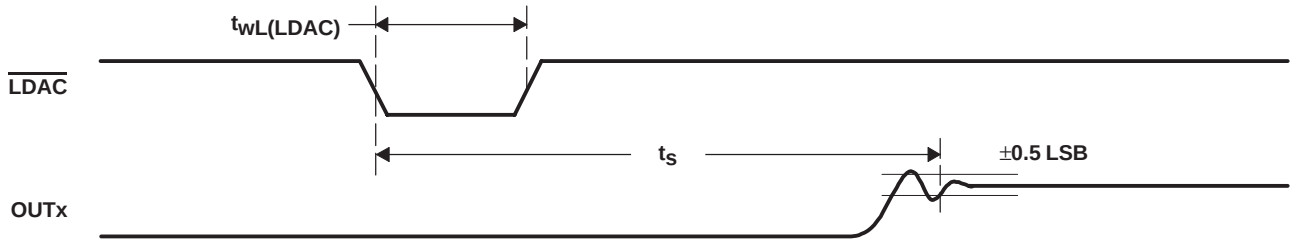


Figure 10. Output Timing

APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5610IYE and TLV5608IYE are 8-channel, 12-bit, single supply DACs, based on a resistor string architecture. They consist of a serial interface, a speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) for each channel is given by:

$$\text{REF}\ \frac{\text{CODE}}{\text{0x1000}}\text{[V]}$$

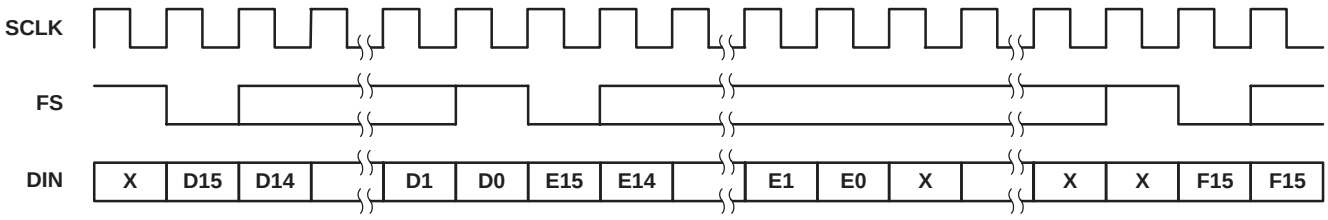
where REF is the reference voltage and CODE is the digital input value. The input range is 0x000 to 0xFFF for the TLV5610IYE and, 0x000 to 0xFFC for the TLV5608IYE. A power on reset initially puts the internal latches to a defined state (all bits zero).

SERIAL INTERFACE

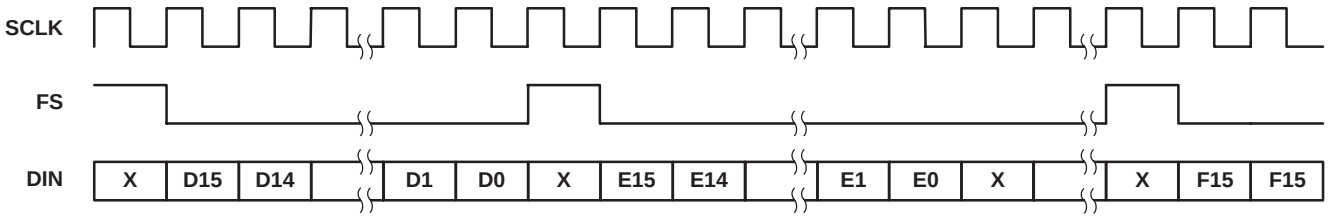
A falling edge of FS starts shifting the data on DIN starting with the MSB to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the content of the shift register is moved to one of the DAC holding registers depending on the address bits within the data word. A logic 0 on the $\overline{\text{LDAC}}$ pin is required to transfer the content of the DAC holding register to the DAC latch and to update the DAC outputs. $\overline{\text{LDAC}}$ is an asynchronous input. It can be held low if a simultaneous update of all eight channels is not needed.

For daisy-chaining, DOUT provides the data sampled on DIN with a delay of 16 clock cycles.

DSP Mode:



µC Mode:



Difference between DSP mode (MODE = N.C. or 0) and µC (MODE = 1) mode:

- In µC mode FS needs to be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge the data transfer is cancelled. The DAC is updated after a rising edge on FS.
- In DSP mode FS only needs to stay low for 20 ns and can go high before the 16th falling clock edge.

SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 30\ MHz$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16\left(t_{whmin} + t_{wlmin}\right)} = 1.95\ MHz$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the DAC has to be considered also.

DATA FORMAT

The 16 bit data word consists of two parts:

- Address bits (D15…D12)
- Data bits (D11…D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	Data											

Ax: Address bits. See table.

REGISTER MAP

A3	A2	A1	A0	FUNCTION
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	0	0	0	CTRL0
1	0	0	1	CTRL1
1	0	1	0	Preset
1	0	1	1	Reserved
1	1	0	0	DAC A and $\overline{B}$
1	1	0	1	DAC C and $\overline{D}$
1	1	1	0	DAC E and $\overline{F}$
1	1	1	1	DAC G and $\overline{H}$

DAC A−H AND TWO-CHANNEL REGISTERS

Writing to DAC A−H sets the output voltage of channel A−H. It is possible to automatically generate the complement of one channel by writing to one of the four two-channel registers (DAC A and $\overline{B}$ etc.).

The TLV5610IYE decodes all 12 data bits. The TLV5608IYE decodes D11 to D2 (D1 and D0 are ignored).

PRESET

The outputs of all DAC channels can be driven to a predefined value stored in the preset register by driving the $\overline{PRE}$ input low. The $\overline{PRE}$ input is asynchronous to the clock.

CTRL0

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	PD	DO	X	X	IM

PD : Full device power down 0 = normal 1 = power down
DO : Digital output enable 0 = disable 1 = enable
IM : Input mode 0 = straight binary 1 = twos complement
X : Reserved

If DOUT is enabled, the data input on DIN is output on DOUT with a 16 cycle delay. That makes it possible to daisy-chain multiple DACs on one serial bus.

CTRL1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	P_{GH}	P_{EF}	P_{CD}	P_{AB}	S_{GH}	S_{EF}	S_{CD}	S_{AB}

P_{XY} : Power Down DAC_{XY} 0 = normal 1 = power down
S_{XY} : Speed DAC_{XY} 0 = slow 1 = fast
XY : DAC pair AB, CD, EF or GH

In power-down mode, the amplifiers of the selected DAC pair within the device are disabled and the total power consumption of the device is significantly reduced. Power-down mode of a specific DAC pair can be selected by setting the PXY bit within the data word to 1.

There are two settling time modes: fast and slow. Fast mode of a DAC pair is selected by setting S_{XY} to 1 and slow mode is selected by setting S_{XY} to 0.

USING TLV5610IYE AND TLV5608IYE, WAFER CHIP SCALE PACKAGE (WCS)

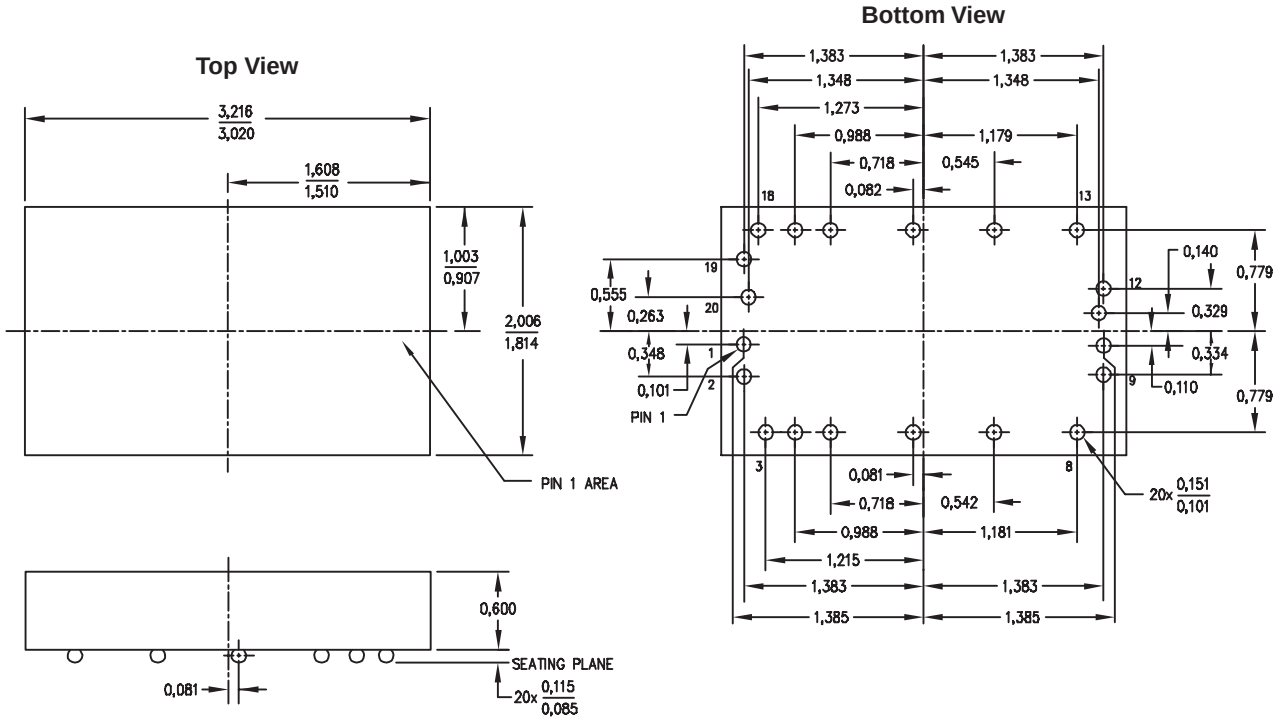
- TLV5610 and TLV5608 qualifications were done using a wire-bonded small outline (SOIC) package and includes: steady state life, thermal shock, ESD, latch-up, biased HAST, autoclave, and characterization. These qualified devices are orderable as TLV5610IDW and TLV5608IDW.
- The wafer chip-scale package (WCS), TLV5610IYE and TLV5608IYE, uses the same DIE as TLV5610IDW and TLV5608IDW respectively, but are not qualified. WCS qualification, including board level reliability (BLR), is the responsibility of the customer.
- It is recommended that underfill be used for increased reliability. BLR is application dependent, but may include test such as: temperature cycling, drop test, key push, bend, vibration, and package shear.

The following WCSP information provides the user of the TLV5610IYE and TLV5608IYE with some general guidelines for board assembly.

- Melting point of eutectic solder is 183°C.
- Recommended peak reflow temperatures are in the 220°C to 230°C range.
- The use of underfill is required. The use of underfill greatly reduces the risk of thermal mismatch fails.

Underfill is an epoxy/adhesive that may be added during the board assembly process to improve board level/system level reliability. The process is to dispense the epoxy under the dice after die attach reflow. The epoxy adheres to the body of the device and to the printed-circuit board. It reduces stress placed upon the solder joints due to the thermal coefficient of expansion (TCE) mismatch between the board and the component. Underfill material is highly filled with silica or other fillers to increase an epoxy's modulus, reduce creep sensitivity, and decrease the material's TCE.

The recommendation for peak flow temperatures of 220°C to 230°C is based on general empirical results that indicate that this temperature range is needed to facilitate good wetting of the solder bump to the substrate or circuit board pad. Lower peak temperatures may cause nonwets (cold solder joints).



NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

Figure 11. TLV5610IYE and TLV5608IYE Wafer Chip Scale Package

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Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
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