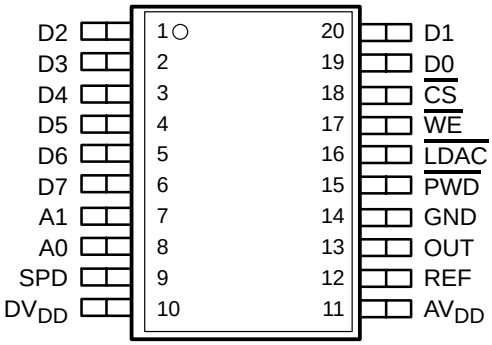
- **12-Bit Voltage Output DAC**
- **Single Supply 2.7-V to 5.5-V Operation**
- **Separate Analog and Digital Supplies**
- **±0.4 LSB Differential Nonlinearity (DNL), ±1.5 LSB Integral Nonlinearity (INL)**
- **Programmable Settling Time vs Power Consumption:**
  1 μs/4.2 mW in Fast Mode,
  3.5 μs/1.2 mW in Slow Mode
- **8-Bit μController Compatible Interface (8+4 Bit)**
- **Power-Down Mode (50 nW)**
- **Rail-to-Rail Output Buffer**
- **Synchronous or Asynchronous Update**
- **Monotonic Over Temperature**

applications

- **Digital Servo Control Loops**
- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Industrial Process Control**
- **Speech Synthesis**
- **Machine and Motion Control Devices**
- **Mass Storage Devices**

DW OR PW PACKAGE
(TOP VIEW)



description

The TLV5613 is a 12-bit voltage output digital-to-analog converter (DAC) with a 8-bit microcontroller compatible parallel interface. The 8 LSBs, the 4 MSBs and 3 control bits are written using three different addresses. Developed for a wide range of supply voltages, the TLV5613 can be operated from 2.7 V to 5.5 V.

The resistor string output voltage is buffered by a x2 gain rail-to-rail output buffer. The buffer features a Class A (slow mode: AB) output stage to improve stability and reduce settling time. The programmable settling time of the DAC allows the designer to optimize speed versus power dissipation. The settling time can be chosen by the control bits within the 16-bit data word.

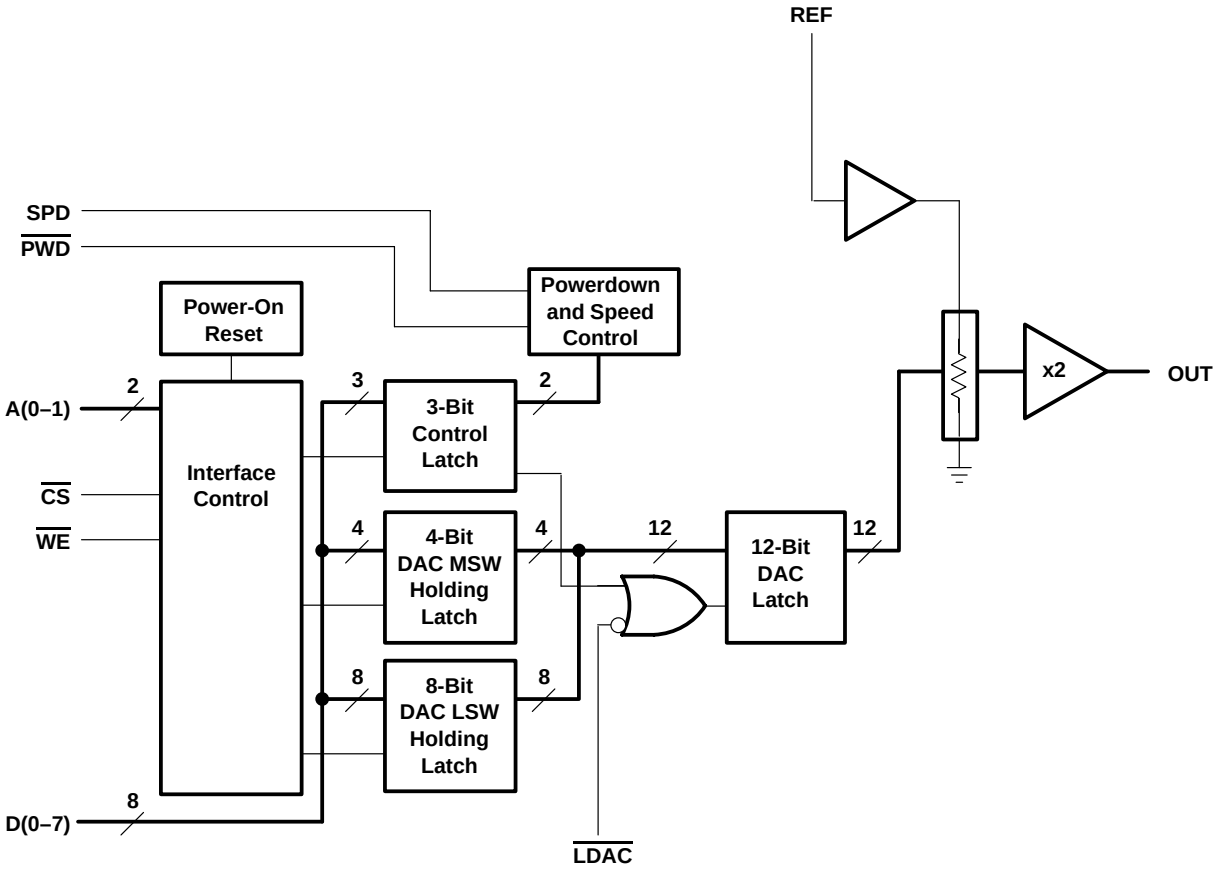
Implemented with a CMOS process, the device is designed for single supply operation from 2.7 V to 5.5 V. It is available in 20 pin SOIC in standard commercial and industrial temperature ranges.

AVAILABLE OPTIONS

PACKAGE		
T_A	SMALL OUTLINE (DW)	TSSOP (PW)
0°C to 70°C	TLV5613CDW	TLV5613CPW
–40°C to 85°C	TLV5613IDW	TLV5613IPW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}	11		Analog positive power supply
A0	8	I	Address input
A1	7	I	Address input
$\overline{CS}$	18	I	Chip select. Digital input active low, used to enable/disable inputs
DV_{DD}	10		Digital positive power supply
D0 (LSB) – D7 (MSB)	1–6, 19, 20	I	Data input
$\overline{LDAC}$	16	I	Load DAC. Digital input active low, used to load DAC output
OUT	13	O	DAC analog voltage output
$\overline{PWD}$	15	I	Power down. Digital input active low
REF	12	I	Analog reference voltage input
SPD	9	I	Speed select. Digital input
GND	14		Ground
$\overline{WE}$	17	I	Write enable. Digital input active low, used to latch data

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (DV_{DD}, AV_{DD} to GND) . . . . . 7 V
Supply voltage difference, AV_{DD} to DV_{DD} . . . . . – 2.8 V to 2.8 V
Reference input voltage range . . . . . – 0.3 V to AV_{DD} + 0.3 V
Digital input voltage range to GND . . . . . – 0.3 V to DV_{DD} + 0.3 V
Operating free-air temperature range, T_A: TLV5613C . . . . . 0°C to 70°C
TLV5613I . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	5-V Supply	4.5	5	5.5	V
	3-V Supply	2.7	3	3.3	
Supply voltage difference, $\Delta V_{DD} = AV_{DD} - DV_{DD}$		–2.8	0	2.8	V
Power on reset, POR		0.55		2	V
High-level digital input voltage, V_{IH}	DV_{DD} = 2.7 V to 5.5 V	2			V
Low-level digital input voltage, V_{IL}	DV_{DD} = 2.7 V to 5.5 V			0.8	V
Reference voltage, V_{ref} to REFIN terminal	5-V Supply (see Note 1)	GND	2.048	AV_{DD}–1.5	V
	3-V Supply (see Note 1)	GND	1.024	AV_{DD}–1.5	
Load resistance, R_L		2			kΩ
Load capacitance, C_L				100	pF
Operating free-air temperature, T_A	TLV5613C	0		70	°C
	TLV5613I	–40		85	°C

NOTE 1: Due to the x2 output buffer, a reference input voltage ≥ (V_{DD} – 0.4)/2 causes clipping of the transfer function.

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

power supply

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs = GND or DV_{DD}, DAC latch = 0x800	V_{DD} = 5 V	Fast		1.6	3	mA
				Slow		0.5	1.3	mA
			V_{DD} = 3 V	Fast		1.4	2.7	mA
				Slow		0.4	1.1	mA
	Power down supply current	See Figure 14				0.01	10	μA
PSRR	Power supply rejection ratio	Zero scale, See Note 2				–65		dB
		Full scale, See Note 3				–65		

NOTES: 2. Power supply rejection ratio at zero scale is measured by varying AV_{DD} and is given by:
$PSRR = 20 \log [(E_{ZS}(AV_{DD}max) – E_{ZS}(AV_{DD}min))/AV_{DD}max]$
3. Power supply rejection ratio at full scale is measured by varying AV_{DD} and is given by:
$PSRR = 20 \log [(E_G(AV_{DD}max) – E_G(AV_{DD}min))/AV_{DD}max]$

static DAC specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V		12			bits
	Integral nonlinearity (INL), end point adjusted	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V,	See Note 4		±1.5	±4	LSB
	Differential nonlinearity (DNL)	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V,	See Note 5		±0.4	±1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V,	See Note 6		±3	±20	mV
	Zero-scale-error temperature coefficient	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V,	See Note 7		3		ppm/°C
E_G	Gain error	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V,	See Note 8		±0.25	±0.5	% of FS voltage
	Gain error temperature coefficient	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V,	See Note 9		1		ppm/°C

NOTES: 4. The relative accuracy or integral nonlinearity (INL) sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
5. The differential nonlinearity (DNL) sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
6. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
7. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = $[E_{ZS}(T_{max}) – E_{ZS}(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.
8. Gain error is the deviation from the ideal output (V_{ref} – 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
9. Gain temperature coefficient is given by: E_G TC = $[E_G(T_{max}) – E_G(T_{min})]/V_{ref} \times 10^6/(T_{max} – T_{min})$.

output specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	R_L = 10 kΩ		0		AV_{DD}–0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 4.096 V,	R_L = 2 kΩ,		0.1	0.29	% of FS voltage
$I_{OSC(source)}$	Output short circuit source current	$V_{O(OUT)}$ = 0 V, input all 1s	AV_{DD} = 5 V		–100		mA
			AV_{DD} = 3 V		–25		
$I_{OSC(sink)}$	Output short circuit sink current	R_L = 100 Ω, input all 1s	AV_{DD} = 5 V		–10		mA
			AV_{DD} = 3 V		–10		

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

reference input (REFIN)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ref}	Input voltage reference	See Note 10		0		$AV_{DD}-1.5$	V
R_i	Input resistance				10		MΩ
C_i	Input capacitance				5		pF
	Reference input bandwidth	REF = 0.2 V_{pp} + 1.024 V dc	Fast mode		1.6		MHz
			Slow mode		1		MHz
	Reference feed through	REF = 1 V_{pp} at 1 kHz + 1.024 V dc, See Note 10			–60		dB

NOTES: 10. Reference feedthrough is measured at the DAC output with an input code = 0x000.

digital inputs

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = DV_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V	–1			µA
C_i	Input capacitance			8		pF

operating characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{s(FS)}$	Output settling time, full scale	R_L = 10 kΩ, C_L = 100 pF,	See Note 11	Fast		1	3	µs
				Slow		3.5	7	
$t_{s(CC)}$	Output settling time, code-to-code	R_L = 10 kΩ, C_L = 100 pF,	See Note 12	Fast		0.5	1.5	µs
				Slow		1	2	
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF,	See Note 13	Fast		8		V/µs
				Slow		1.5		
	Glitch energy	Code-to-code transition				1		nV–s
S/N	Signal-to-noise	f_S = 480 KSPS, R_L = 10 k,	f_{out} = 1 kHz, C_L = 100 pF		65	78		dB
S/(N+D)	Signal-to-noise + distortion				58	69		
THD	Total harmonic distortion					–68	–60	
	Spurious free dynamic range				60	72		

NOTES: 11. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0x3FF or 0x3FF to 0x020.
12. Settling time is the time for the output signal to remain within ± 0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full scale.
13. Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full-scale voltage.

timing requirements

digital inputs

		MIN	NOM	MAX	UNIT
$t_{su(D)}$	Setup time, data ready before positive $\overline{WE}$ edge	9			ns
$t_{su(CS-WE)}$	Setup time, $\overline{CS}$ low before positive $\overline{WE}$ edge	13			ns
$t_{su(A)}$	Setup time, address bits A0, A1	17			ns
$t_{h(D)}$	Hold time, data held after positive $\overline{WE}$ edge	0			ns
$t_{su(WE-LD)}$	Setup time, positive $\overline{WE}$ edge before $\overline{LDAC}$ low	0			ns
$t_{w(WE)}$	Pulse duration, $\overline{WE}$ high	25			ns
$t_{w(LD)}$	Pulse duration, $\overline{LDAC}$ low	25			µs

PARAMETER MEASUREMENT INFORMATION

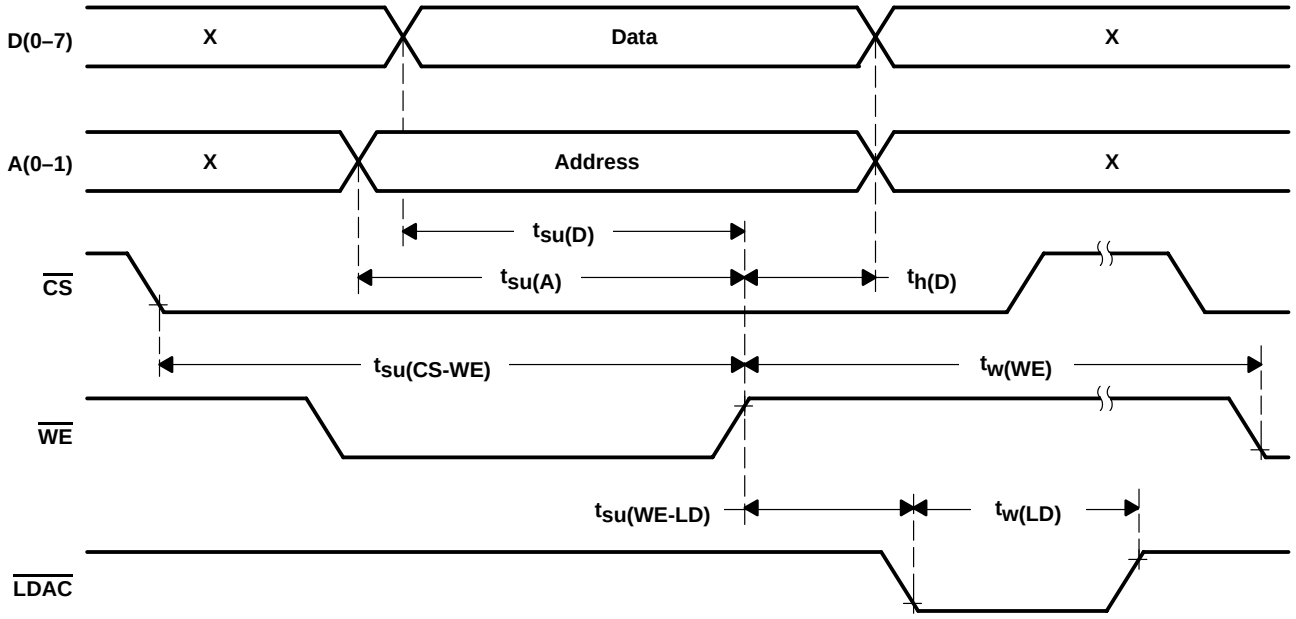


Figure 1. Timing Diagram

PARAMETER MEASUREMENT INFORMATION

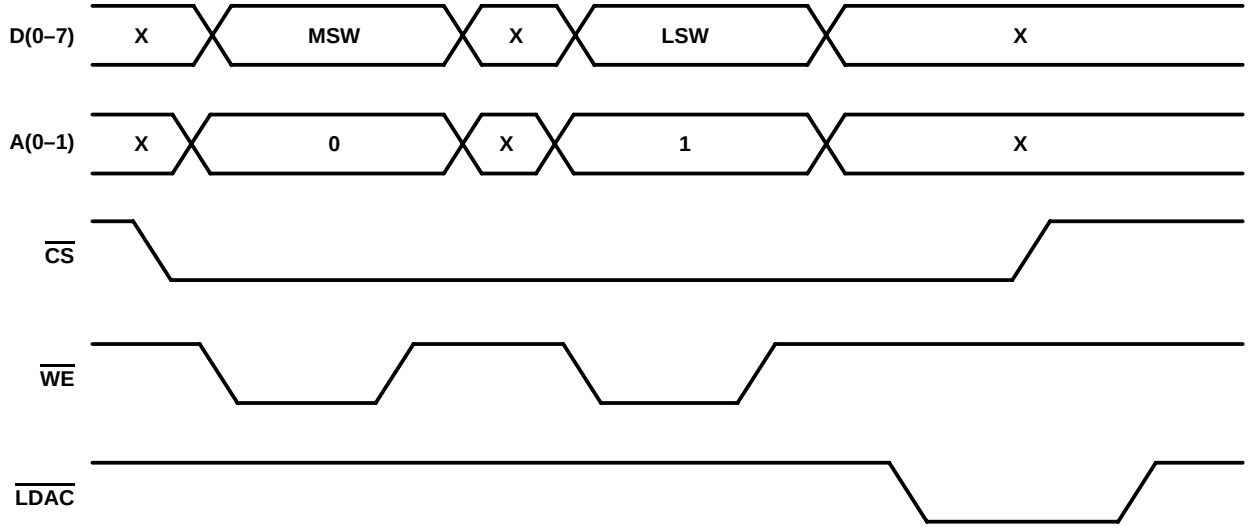


Figure 2. Example of a Complete Write Cycle Using $\overline{\text{LDAC}}$ to Update the DAC

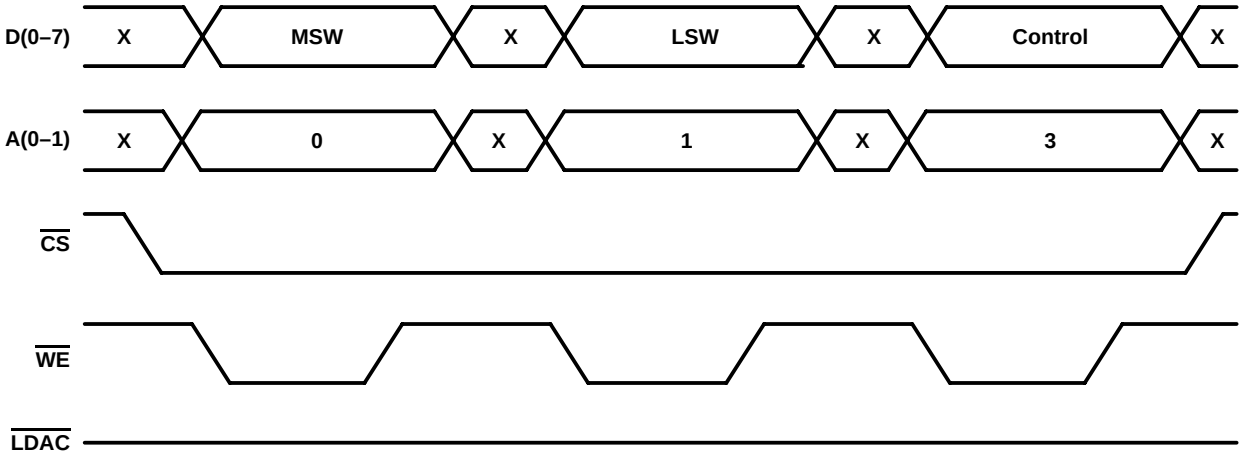


Figure 3. Example of a Complete Write Cycle Using the Control Word to Update the DAC

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE
vs
LOAD

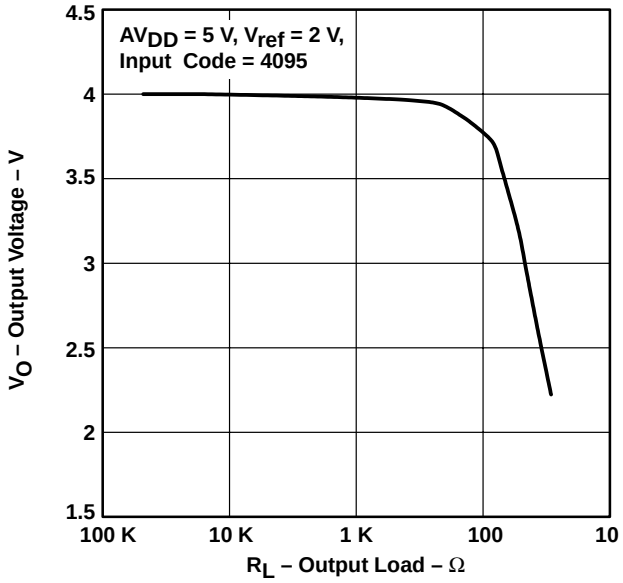


Figure 4

MAXIMUM OUTPUT VOLTAGE
vs
LOAD

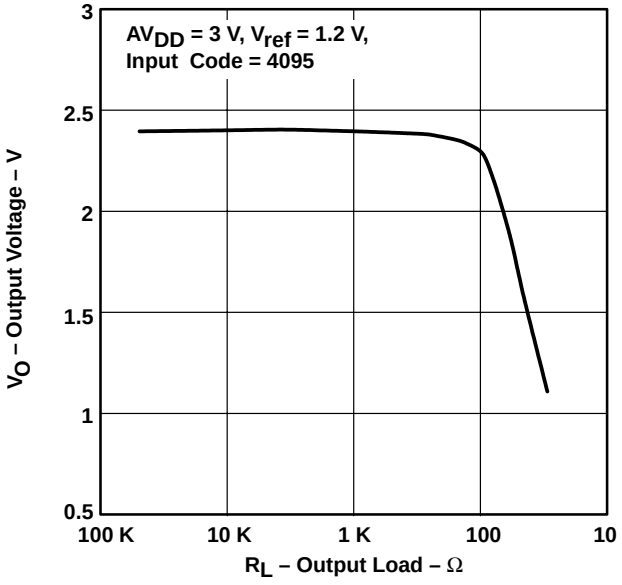


Figure 5

TOTAL HARMONIC DISTORTION
vs
LOAD

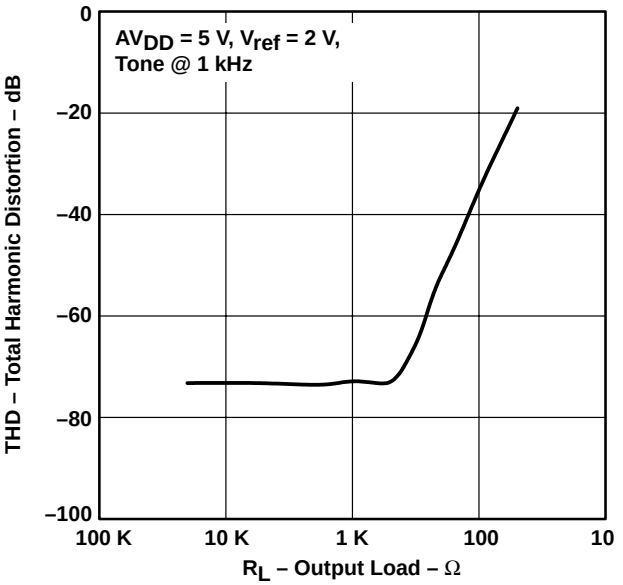


Figure 6

TOTAL HARMONIC DISTORTION
vs
LOAD

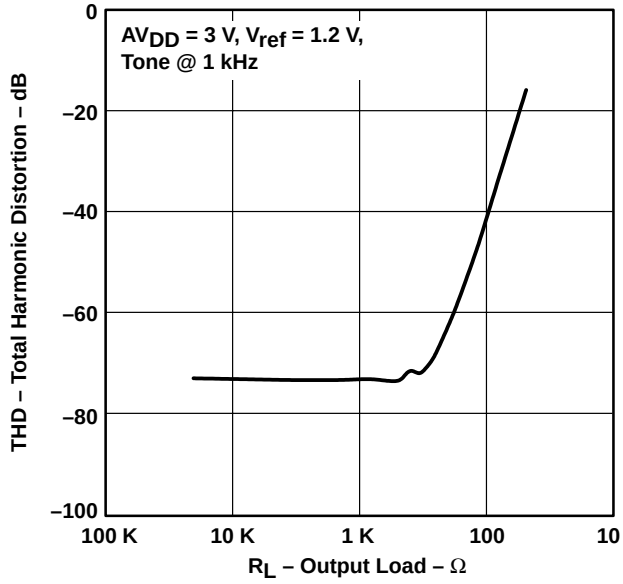


Figure 7

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs FREQUENCY

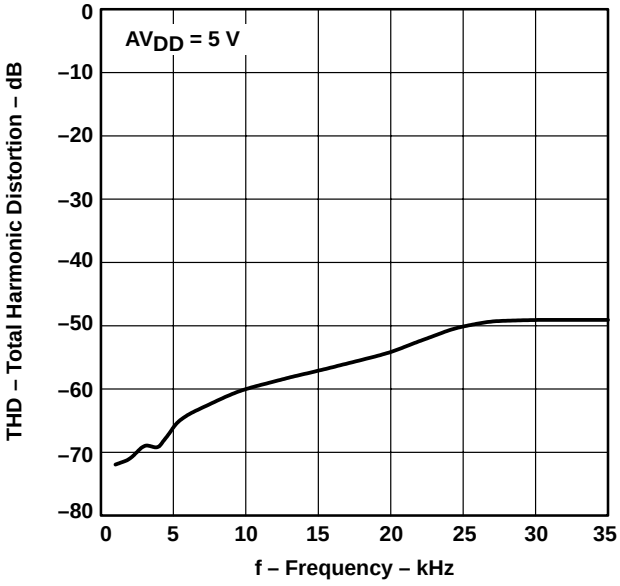


Figure 8

TOTAL HARMONIC DISTORTION vs FREQUENCY

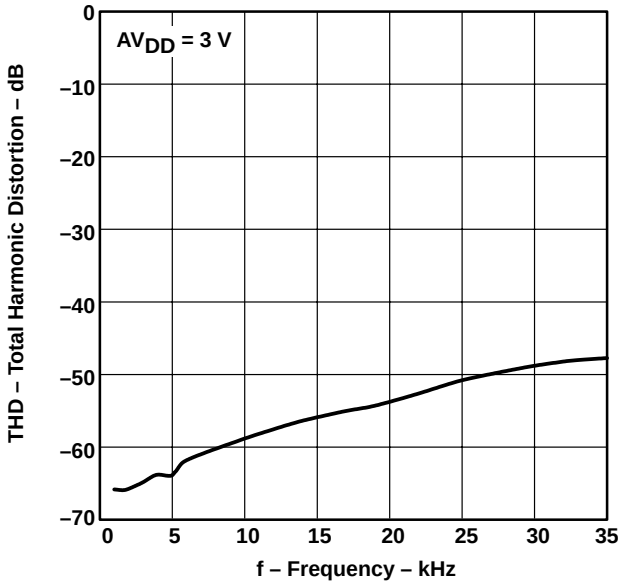


Figure 9

SIGNAL-TO-NOISE + DISTORTION vs FREQUENCY

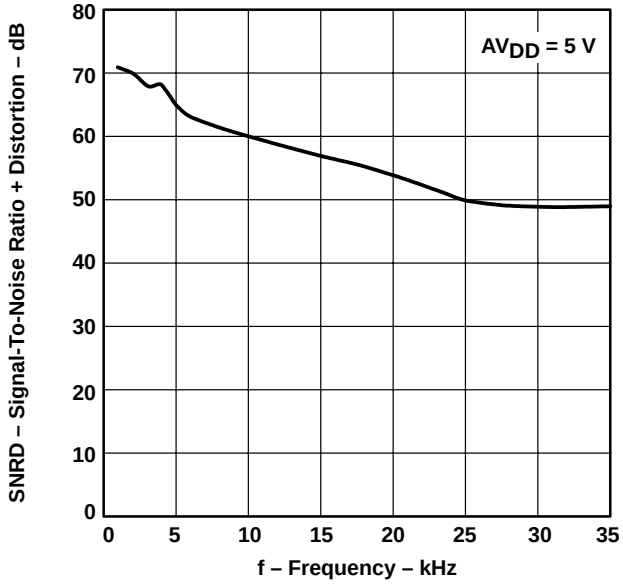


Figure 10

SIGNAL-TO-NOISE + DISTORTION vs FREQUENCY

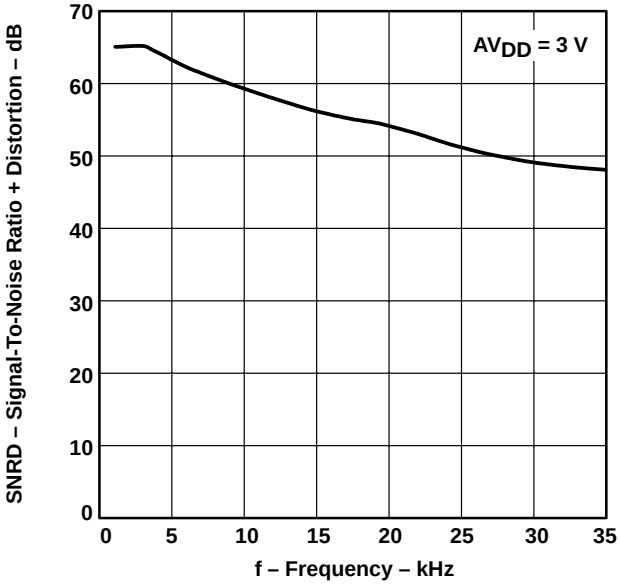


Figure 11

TYPICAL CHARACTERISTICS

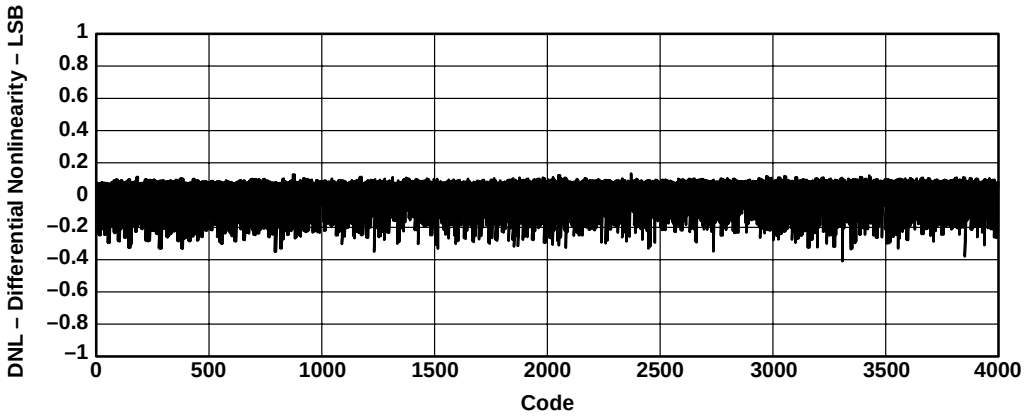


Figure 12. Differential Nonlinearity

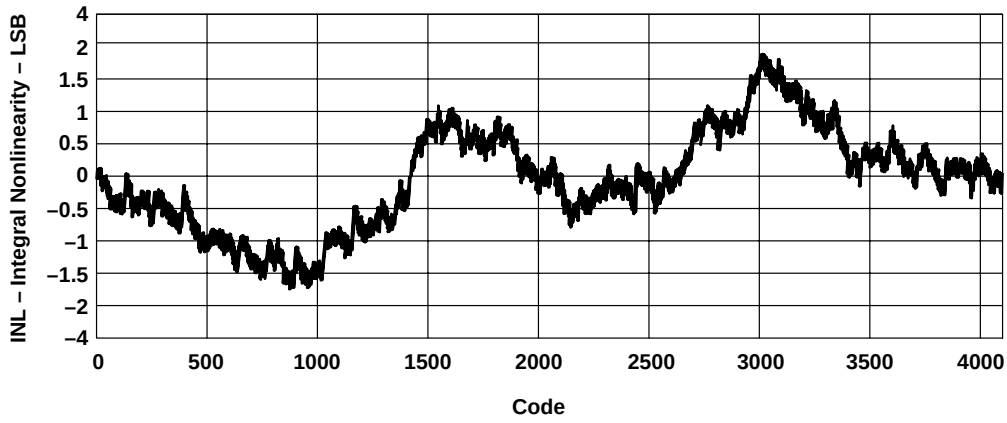


Figure 13. Integral Nonlinearity

TYPICAL CHARACTERISTICS

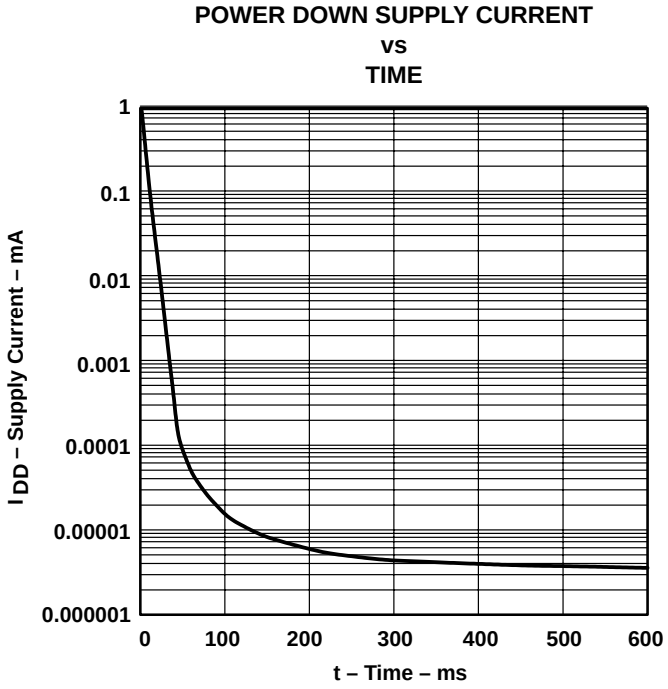


Figure 14

APPLICATION INFORMATION

general function

The TLV5613 is a 12-bit, single supply DAC, based on a resistor string architecture. It consists of a parallel interface, speed and power down control logic, a resistor string and a rail-to-rail output buffer. The output voltage (full scale determined by reference) is given by:

$$2 \text{ REF } \frac{\text{CODE}}{\text{0x1000}} \text{ [V]}$$

Where REF is the reference voltage and CODE is the digital input value, range 0x000 to 0xFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

parallel interface

The device latches data on the positive edge of $\overline{\text{WE}}$. It must be enabled with $\overline{\text{CS}}$ low. Whether the data is written to one of the DAC holding latches (MSW, LSW) or the control register, depends on the address bits A1 and A0. $\overline{\text{LDAC}}$ low updates the DAC with the value in the holding latch. $\overline{\text{LDAC}}$ is an asynchronous input and can be held low, if a separate update is not necessary. Two more asynchronous inputs, SPD and $\overline{\text{PWD}}$ control the settling times and the power down mode:

SPD:	Speed control	1 → fast mode	0 → slow mode
$\overline{\text{PWD}}$:	Power control	1 → normal operation	0 → power down

APPLICATION INFORMATION

It is also possible to program the different modes (fast, slow, power down) and the DAC update latch using the control register. The following tables list the possible combination of the control signals and control bits.

PIN	BIT	MODE
SPD	SPD	
0	0	Slow
0	1	Fast
1	0	Fast
1	1	Fast

PIN	BIT	POWER
$\overline{\text{PWD}}$	PWD	
0	0	Down
0	1	Down
1	0	Normal
1	1	Down

PIN	BIT	LATCH
$\overline{\text{LDAC}}$	RLDAC	
0	0	Transparent
0	1	Transparent
1	0	Hold
1	1	Transparent

data format

The TLV5613 writes data either to one of the DAC holding latches or to the control register depending on the address bits A1 and A0.

ADDRESS BITS

A1	A0	REGISTER
0	0	DAC LSW holding
0	1	DAC MSW holding
1	0	Reserved
1	1	Control

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	RLDAC	PWD	SPD

X: Don't care
SPD: Speed control bit 1 → fast mode 0 → slow mode
PWD: Power control bit 1 → power down 0 → normal operation
RLDAC: Load DAC latch 1 → latch transparent 0 → DAC latch controlled by $\overline{\text{LDAC}}$ pin

APPLICATION INFORMATION

layout considerations

To achieve the best performance, it is recommended to have separate power planes for GND, AV_{DD}, and DV_{DD}. Figure 15 shows how to lay out the power planes for the TLV5613. As a general rule, digital and analog signals should be separated as wide as possible. To avoid crosstalk, analog and digital traces must not be routed in parallel. The two positive power planes (AV_{DD} and DV_{DD}) should be connected together at one point with a ferrite bead.

A 100-nF ceramic low series inductance capacitor between DV_{DD} and GND and a 1-µF tantalum capacitor between AV_{DD} and GND as close as possible to the supply pins are recommended for optimal performance.

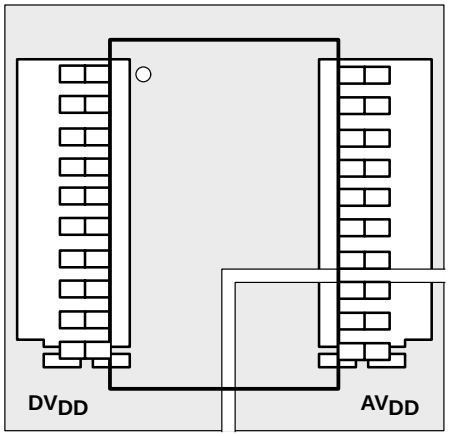


Figure 15. TLV5613 Board Layout

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 16.

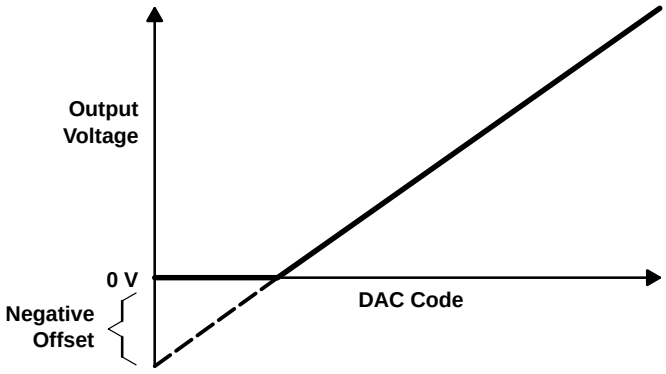


Figure 16. Effect of Negative Offset (Single Supply)

APPLICATION INFORMATION

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage.

TLV5613 interfaced to an Intel MCS®251 controller

The circuit in Figure 17 shows how to interface the TLV5613 to an Intel MCS®251 microcontroller. The address bus and the data bus of the controller are multiplexed on port 0 (non page mode) to save port pins. To separate the address bits and the data bits, the controller provides a dedicated signal, address latch enable (ALE), which is connected to a latch at port 0.

An address decoder is required to generate the chip select signal for the TLV5613. In this example, a simple 3-to-8 decoder (74AC138) is used for the interface as shown in Figure 17. The DAC is memory mapped at addresses 0x8000/1/2/3 within the data memory address space and mirrored every 32 address locations (0x8020/1/2/3, 0x8040/1/2/3, etc.). In a typical microcontroller system, programmable logic should be used to generate the chip select signals for the entire system.

The data pins and the $\overline{WE}$ pin of the TLV5613 can be connected directly to the multiplexed address and data bus and the $\overline{WR}$ signal of the controller.

$\overline{LDAC}$ is held high so that the output voltage is updated using the RLDAC bit in the control register. Hardware power down mode is deactivated permanently by pulling $\overline{PWD}$ to DV_{DD}.

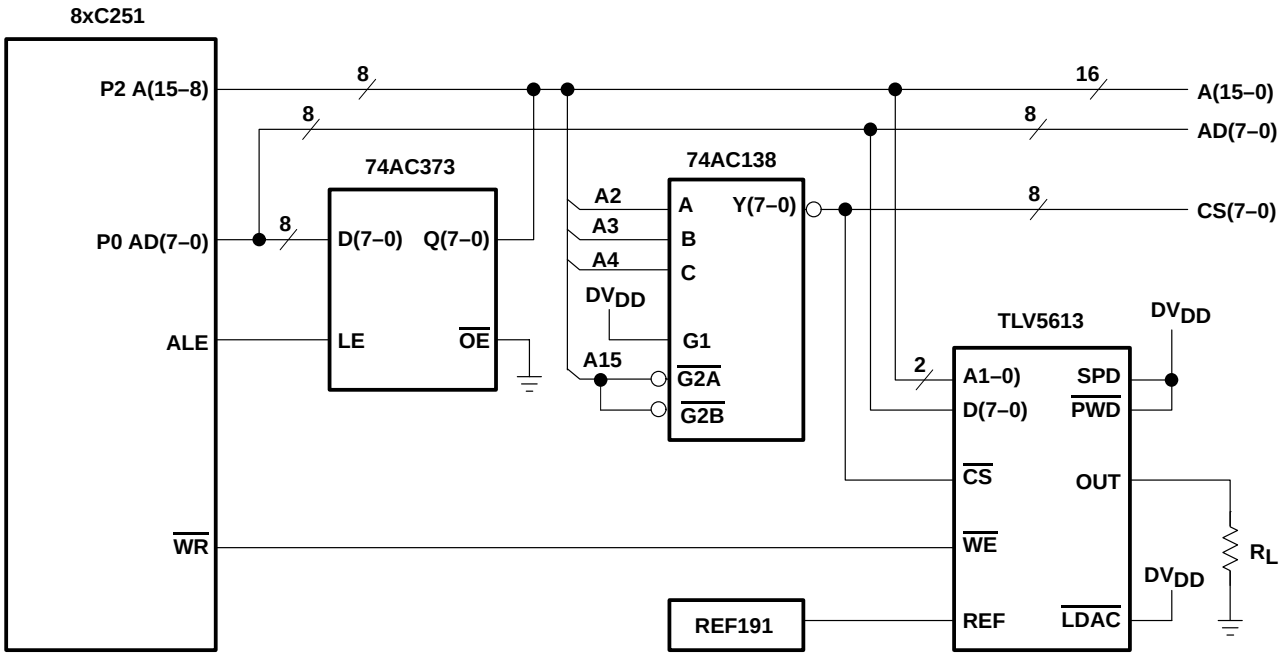


Figure 17. TLV5613 Interfaced to an Intel MCS®251 Controller

MCS is a registered trademark of Intel Corporation.

APPLICATION INFORMATION

software

In the following example, the code generates a waveform at 500 KSPS with 500 samples stored in a table within the program memory space of the microcontroller. The period of the waveform is 1 ms.

The waveform data is located in the program memory space from address 01000h to address 013E8h ($2 \times 500 = 1000 = 03E8h$) beginning with the MSW of the first 16-bit word (the 4 MSBs are ignored), followed by the LSW. Two bytes are required for each DAC word (the table is not shown in the code example).

The program consists of two parts:

- A main routine, which is executed after reset and which initializes the timer and the interrupt system of the microcontroller.
- An interrupt service routine, which reads a new value from the waveform table and writes it to the DAC.

This example uses timer 0 in mode 3 (8-bit timer with auto reload). The clock of the timer is derived from the system clock and has a frequency of $f_{osc}/12$. The timer overrun frequency f_{tim} is given by the following equation:

$$f_{tim} = \frac{f_{OSC}}{12(256-Reload)} \text{ and the reload value is given by } Reload = 256 - \frac{f_{OSC}}{12\ f_{tim}}$$

To get a timer overrun frequency of 500 kHz at a system clock of 24 MHz, the reload value is:

$$Reload = 256 - \frac{24}{12 \times 0.5} = 256-4 = 252 = 0FCh$$

With this value, the timer generates an interrupt every 2 μs. The corresponding service routine `T0_isr` reads a sample from program memory and writes it to the DAC. First, it disables the update of the DAC output by clearing the RLDAC bit in the control register. Then it reads the MSW and the LSW from the waveform table and stores it in the MSW and LSW register of the TLV5613. The write cycle is completed by setting the RLDAC bit, which updates the DAC output. At the end of the interrupt service routine, the pointer to the waveform samples is increased and is checked to determine if it has reached the end of the table. If the pointer has reached the end of the table, the pointer is set to the start address of the table.

APPLICATION INFORMATION

```
;*********************************************************************
;* Title  : Waveform generation with TLV5613                         *
;* Version: 1.0                                                      *
;* MCU    : Intel MCS®251, MCS®51                                     *
;* © 1998 Texas Instruments Inc.                                     *
;*********************************************************************

TABLE_START EQU 01000h            ;start address of waveform data
TABLE_END_H EQU 013h              ;high byte – end address of waveform data
TABLE_END_L EQU 0E8h              ;low byte  – end address of waveform data
RELOAD      EQU 0FCh              ;timer reload value

            ORG 00000h            ;entry point
            JMP main              ;jump to main program
            ORG 0000bh            ;timer0 (T0) interrupt vector
            JMP T0_isr            ;jump to T0 interrupt service routine

;---------------------------------------------------------------------
;main: setup timer and interrupt, loop forever
;---------------------------------------------------------------------
main:       CLR A
            MOV A, IE0            ;disable all interrupts
            CLR TCON.4            ;stop T0
            MOV A, #002h
            MOV TMOD, A           ;set T0 to auto reload mode
            MOV A, #RELOAD
            MOV TH0, A            ;set T0 reload value
            MOV TL0, A            ;set T0 start value
            MOV P2, #080h         ;set A15 of address bus to select DAC

            MOV DPTR, #TABLE_START ;set data pointer to start of wave form data

            SETB IE0.1            ;enable T0 interrupt
            SETB IE0.7            ;enable interrupts
            SETB TCON.4           ;start T0
idle_loop:  SJMP idle_loop        ;loop forever
```

APPLICATION INFORMATION

```
;-------------------------------------------------------------------------
;T0_isr: will be called on every timer interrupt.
;fetches a new 16–bit value from program memory space and writes it
;to the DAC. If end of table is reached, sets DPTR to table start addr.
;-------------------------------------------------------------------------
T0_isr:     MOV R0, #003h          ;select DAC control register
            MOV A, #001h           ;RLDAC=0, PWD=0, SPD=1
                                   ;no DAC update, normal operation, fast mode
            MOVX @R0, A            ;write Accu to DAC control register

            MOV R0, #001h          ;select DAC MSW register
            CLR A
            MOVC A, @A+DPTR        ;get MSW from code memory
            MOVX @R0, A            ;write Accu to DAC MSW register

            INC DPTR               ;set DPTR to LSW data

            MOV R0, #000h          ;select DAC LSW register
            CLR A
            MOVC A, @A+DPTR        ;get LSW from code memory
            MOVX @R0, A            ;write Accu to DAC LSW register

            MOV R0, #003h          ;select DAC control register (to update DAC)
            MOV A, #005h           ;DAC update, normal operation, fast mode
            MOVX @R0, A            ;write Accu to DAC control register

            INC DPTR               ;set DPTR to next MSW
                                   ;test end of table
            MOV A, DPL
            CJNE A, #TABLE_END_L, T0_isr_end
            MOV A, DPH
            CJNE A, #TABLE_END_H, T0_isr_end
            MOV DPTR, #TABLE_START ;end of table reached –> start again
T0_isr_end: RETI

            END
```

APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (SINAD)

Signal-to-noise ratio + distortion is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

spurious free dynamic range (SFDR)

Spurious free dynamic range is the difference between the rms value of the output signal and the rms value of the spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

Total harmonic distortion is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV5613CDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5613C	Samples
TLV5613CDWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TLV5613C	Samples
TLV5613CPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TV5613	Samples
TLV5613IDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5613I	Samples
TLV5613IDWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5613I	Samples
TLV5613IDWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TLV5613I	Samples
TLV5613IPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5613	Samples
TLV5613IPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5613	Samples
TLV5613IPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY5613	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

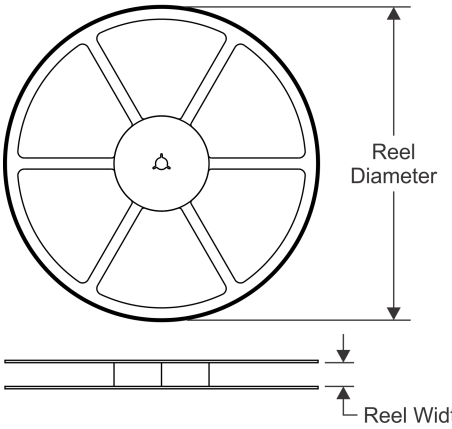
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

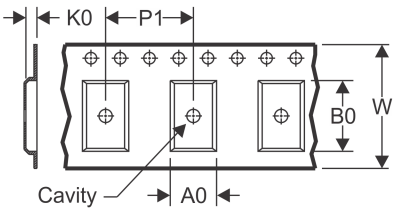
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

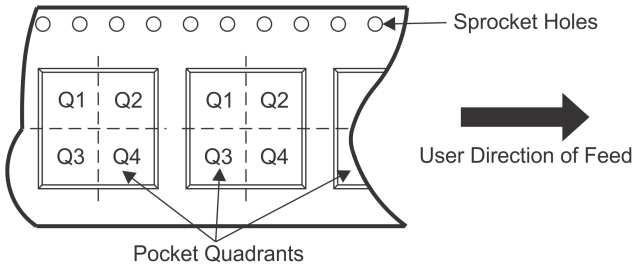


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

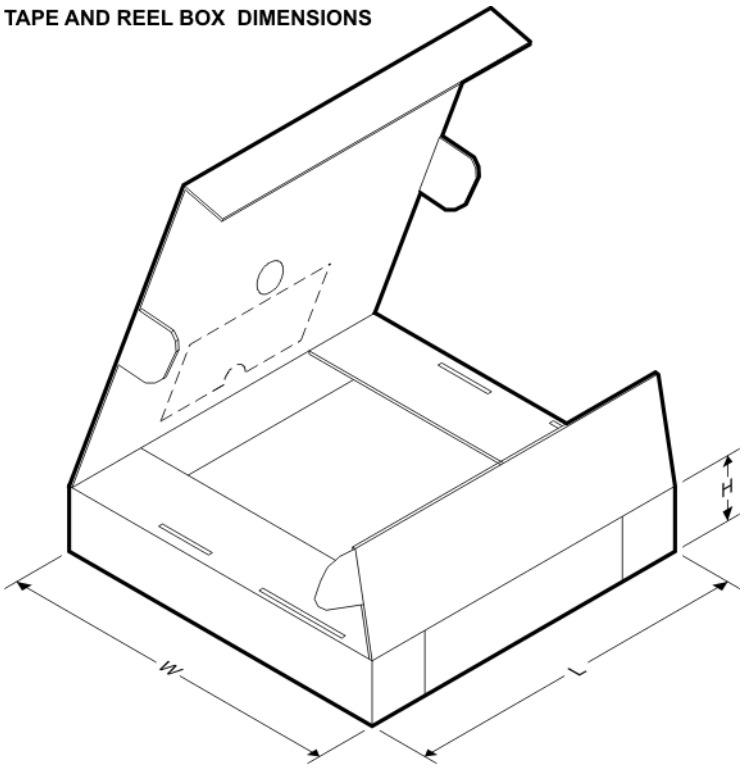
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV5613IDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TLV5613IPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV5613IDWR	SOIC	DW	20	2000	367.0	367.0	45.0
TLV5613IPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

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