TMS320VC5441 Fixed-Point Digital Signal Processor

Data Manual

Literature Number: SPRS122F
December 1999 − Revised October 2008

TEXAS INSTRUMENTS

REVISION HISTORY

This data sheet revision history highlights the technical changes made to the SPRS122E device-specific data sheet to make it an SPRS122F revision.

Scope: This document has been reviewed for technical accuracy; the technical content is up-to-date as of the specified release date with the following changes.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
17	Table 2−3, Signal Descriptions: − Updated DESCRIPTION of $\overline{\text{TRST}}$ − Added footnote about $\overline{\text{TRST}}$
85	Section 6, Mechanical Data: − Moved “Package Thermal Resistance Characteristics” section (Section 5.4 in SPRS122E) to Section 6.1 − Added Section 6.2, Packaging Information − Mechanical drawings will be appended to this document via an automated process

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1 TMS320VC5441 Features

- **532-MIPS Quad-Core DSP Consisting of Four Independent Subsystems**
- **Each Core has an Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Bus**
- **40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel-Shifter and Two 40-Bit Accumulators Per Core**
- **Each Core has a 17-Bit × 17-Bit Parallel Multiplier Coupled to a 40-Bit Adder for Non-Pipelined Single-Cycle Multiply/ Accumulate (MAC) Operations**
- **Each Core has a Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Each Core has an Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Each Core has Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Total 640K-Word × 16-Bit Dual-Access On-Chip RAM (256K-Word x 16-Bit Shared Memory and 96K-Word x 16-Bit Local Memory Per Subsystem)**
- **Single-Instruction Repeat and Block-Repeat Operations**
- **Instructions With 32-Bit Long Word Operands**
- **Instructions With 2 or 3 Operand Reads**
- **Fast Return From Interrupts**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
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- **Dual 1.6-V (Core) and 3.3-V (I/O) Power Supplies for Low-Power, Fast Operations**
- **7.5-ns Single-Cycle Fixed-Point Instruction**
- **Twenty-Four Channels of Direct Memory Access (DMA) for Data Transfers With No CPU Loading (Six Channels Per Subsystem)**
- **Twelve Multichannel Buffered Serial Ports (McBSPs), Each With 128-Channel Selection Capability (Three McBSPs per Subsystem)**
- **16-Bit Host-Port Interface (HPI)**
- **Software-Programmable Phase-Locked Loop (PLL) Provides Several Clocking Options (Requires External TTL Oscillator)**
- **On-Chip Scan-Based Emulation Logic, IEEE Standard 1149.1† (JTAG) Boundary-Scan Logic**
- **Four Software-Programmable Timers (One Per Subsystem)**
- **Four Software-Programmable Watchdog Timers (One Per Subsystem)**
- **Sixteen General-Purpose I/Os (Four Per Subsystem)**
- **Provided in 176-pin Plastic Low-Profile Quad Flatpack (LQFP) Package (PGF Suffix)**
- **Provided in 169-ball MicroStar BGA™ Package (GGU Suffix)**

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† IEEE Standard 1149.1-1990, Standard Test-Access Port and Boundary Scan Architecture.

2 Introduction

This section describes the main features of the TMS320VC5441 digital signal processor (DSP), lists the pin assignments, and describes the function of each pin. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

NOTE: This data manual is designed to be used in conjunction with the *TMS320C54x™ DSP Functional Overview* (literature number SPRU307).

2.1 Description

The TMS320VC5441 fixed-point digital signal processor is a quad-core solution running at 532-MIPS performance. The 5441 consists of four DSP subsystems with shared program memory. Each subsystem consists of one TMS320C54x™ DSP core, 32K-word program/data DARAM, 64K-word data DARAM, three multichannel buffered serial ports, DMA logic, one watchdog timer, one general-purpose timer, and other miscellaneous circuitry.

The 5441 also contains a host-port interface (HPI) that allows the 5441 to be viewed as a memory-mapped peripheral to a host processor.

Each subsystem has its separate program and data spaces, allowing simultaneous accesses to program instructions and data. Two read operations and one write operation can be performed in one cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. Furthermore, data can be transferred between program and data spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. The 5441 includes the control mechanisms to manage interrupts, repeated operations, and function calls. In addition, the 5441 has a total of 256K words of shared program memory (128K words shared by subsystems A and B, and another 128K words shared by subsystems C and D).

The 5441 is intended as a high-performance, low-cost, high-density DSP for remote data access or voice-over IP subsystems. It is designed to maintain the current modem architecture with minimal hardware and software impacts, thus maximizing reuse of existing modem technologies and development efforts.

The 5441 is offered in two temperature ranges and individual part numbers are shown below. (Please note that the industrial temperature device part numbers do not follow the typical numbering tradition.)

Commercial temperature devices (0°C to 85°C)
- TMS320VC5441PGF532 (176-pin LQFP)
- TMS320VC5441GGU532 (169-ball BGA)

Industrial temperature range devices (−40°C to 100°C)
- TMS320VC5441APGF532 (176-pin LQFP)
- TMS320VC5441AGGU532 (169-ball BGA)

NOTE: Leading “x” in signal names identifies the subsystem; x = A, B, C, or D for subsystem A, B, C, or D, respectively. Trailing “n” in signal names identifies the McBSP; n = 0, 1, or 2 for McBSP0, McBSP1, or McBSP2, respectively.

TMS320C54x is a trademark of Texas Instruments.

2.2 Migration From the 5421 to the 5441

Customers who are migrating from the 5421 to the 5441 need to take into account the following differences between the two devices.

- The 5441 provides four cores in a 169-ball ball grid array (BGA) and a 176-pin low-profile quad flatpack (LQFP).
- The 5441 does not have a XIO interface for external memory connection.
- Each subsystem includes a 32K-word DARAM program/data memory and a 64K-word DARAM data memory.
- The DMA has been changed and now provides no access to external memory.
- The HPI and DMA memory maps have been changed to incorporate the new 5441 memory structure.
- The 2K words of ROM on the 5421 is not implemented on the 5441.
- The four McBSP1s and four McBSP2s have been internally multiplexed onto two sets of external pins.
- The HPI_SEL1 and HPI_SEL2 pins on 5441 are used to facilitate HPI module selection among the four subsystems.
- The 5441 provides four watchdog timers (one per subsystem).
- GPIO0 and GPIO1 pins are multiplexed with x_XF and x_BIO pins, respectively.
- Only the global reset ($\overline{\text{RESET}}$) will reset the PLL.

2.3 Pin Assignments

Figure 2−1 illustrates the ball locations for the 169-ball ball grid array (BGA) package and is used in conjunction with Table 2−1 to locate signal names and ball grid numbers. Figure 2−2 illustrates the pin locations for the 176-pin low-profile quad flatpack (LQFP); Table 2−2 lists each pin number and its associated pin name for this package.

2.3.1 Pin Assignments for the GGU Package

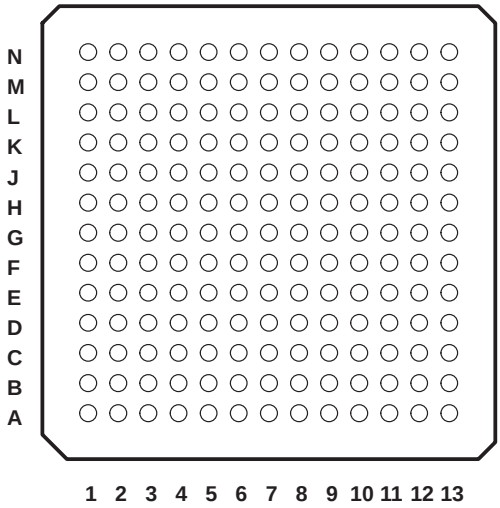


Figure 2−1. 169-Ball GGU MicroStar BGA™ (Bottom View)

Table 2−1. Pin Assignments for TMS320VC5441GGU (169-Ball BGA Package)†

BALL #	SIGNAL NAME	BALL #	SIGNAL NAME	BALL #	SIGNAL NAME	BALL #	SIGNAL NAME
A1	HA[0]/HCNTL0	A2	DV_{DD}	A3	V_{SS}	A4	B_BDR0
A5	CV_{DD}	A6	V_{SS}	A7	DV_{DD}	A8	V_{SS}
A9	CV_{DD}	A10	D_BDR0	A11	V_{SS}	A12	DV_{DD}
A13	D_BFSX0	B1	HA[1]/HCNTL1	B2	B_BFSX0	B3	B_BFSR0
B4	B_BDX0	B5	CV_{DD}	B6	HD[7]	B7	HD[3]
B8	HD[0]	B9	CV_{DD}	B10	D_GPIO0/D_XF	B11	D_BDX0
B12	D_BFSR0	B13	HA[18]	C1	V_{SS}	C2	HA[3]/$\overline{\text{B\_HINT}}$
C3	B_GPIO1/$\overline{\text{B\_BIO}}$	C4	B_GPIO0/B_XF	C5	CV_{DD}	C6	B_BCLKR0
C7	HD[4]	C8	D_GPIO3/D_TOUT	C9	CV_{DD}	C10	D_BCLKX0
C11	HA[17]	C12	HA[15]	C13	V_{SS}	D1	CLKMD
D2	$\overline{\text{B\_NMI}}$	D3	$\overline{\text{B\_RS}}$	D4	HA[4]/$\overline{\text{C\_HINT}}$	D5	CV_{DD}
D6	B_BCLKX0	D7	HD[5]	D8	D_GPIO1/$\overline{\text{D\_BIO}}$	D9	CV_{DD}
D10	D_BCLKR0	D11	$\overline{\text{D\_RS}}$	D12	$\overline{\text{D\_INT}}$	D13	$\overline{\text{TRST}}$
E1	DV_{DD}	E2	TESTB	E3	TDI	E4	$\overline{\text{B\_INT}}$
E5	HA[2]/$\overline{\text{A\_HINT}}$	E6	B_GPIO3/B_TOUT	E7	HD[6]	E8	HD[1]
E9	D_GPIO2/$\overline{\text{D\_WTOUT}}$	E10	TESTD	E11	TMS	E12	TCK
E13	DV_{DD}	F1	V_{SSA}	F2	V_{SS}	F3	$\overline{\text{HCS}}$
F4	$\overline{\text{HAS}}$	F5	CLKIN	F6	B_GPIO2/$\overline{\text{B\_WTOUT}}$	F7	HD[2]
F8	HA[16]	F9	$\overline{\text{D\_NMI}}$	F10	EMU1/$\overline{\text{OFF}}$	F11	HPI_SEL2
F12	HPI_SEL1	F13	V_{SS}	G1	V_{CCA}	G2	CV_{DD}
G3	EMU0	G4	BCLKR2	G5	BCLKX2	G6	HRDY
G7	BDR1	G8	HMODE	G9	$\overline{\text{HDS2}}$	G10	$\overline{\text{C\_NMI}}$
G11	$\overline{\text{RESET}}$	G12	HR/$\overline{\text{W}}$	G13	CV_{DD}	H1	V_{SS}
H2	BFSR2	H3	BFSX2	H4	CLKOUT	H5	$\overline{\text{A\_INT}}$
H6	HA[7]	H7	HD[9]	H8	C_GPIO1/$\overline{\text{C\_BIO}}$	H9	BCLKX1
H10	BCLKR1	H11	BFSR1	H12	BFSX1	H13	V_{SS}
J1	DV_{DD}	J2	BDR2	J3	BDX2	J4	$\overline{\text{A\_RS}}$
J5	A_GPIO1/$\overline{\text{A\_BIO}}$	J6	HD[8]	J7	HD[13]	J8	C_BCLKR0
J9	HA[11]	J10	$\overline{\text{C\_INT}}$	J11	$\overline{\text{C\_RS}}$	J12	BDX1
J13	DV_{DD}	K1	V_{SS}	K2	$\overline{\text{A\_NMI}}$	K3	TDO
K4	A_GPIO3/A_TOUT	K5	CV_{DD}	K6	A_GPIO2/$\overline{\text{A\_WTOUT}}$	K7	HD[12]
K8	C_BCLKX0	K9	CV_{DD}	K10	HA[13]	K11	HA[14]
K12	TESTC	K13	$\overline{\text{HDS1}}$	L1	HA[5]/$\overline{\text{D\_HINT}}$	L2	HA[6]
L3	HA[8]	L4	A_GPIO0/A_XF	L5	CV_{DD}	L6	A_BCLKR0
L7	HD[11]	L8	HD[15]	L9	CV_{DD}	L10	C_GPIO0/C_XF
L11	C_GPIO2/$\overline{\text{C\_WTOUT}}$	L12	HA[12]	L13	V_{SS}	M1	V_{SS}
M2	HA[9]	M3	A_BFSR0	M4	A_BDR0	M5	CV_{DD}
M6	A_BCLKX0	M7	HD[10]	M8	HD[14]	M9	CV_{DD}
M10	C_GPIO3/C_TOUT	M11	C_BDX0	M12	C_BFSR0	M13	HA[10]
N1	A_BFSX0	N2	DV_{DD}	N3	V_{SS}	N4	A_BDX0
N5	CV_{DD}	N6	V_{SS}	N7	DV_{DD}	N8	V_{SS}
N9	CV_{DD}	N10	C_BDR0	N11	V_{SS}	N12	DV_{DD}
N13	C_BFSX0						

† Cells highlighted in gray indicate pins that perform a multiplexed function.

2.3.2 Pin Assignments for the PGF Package

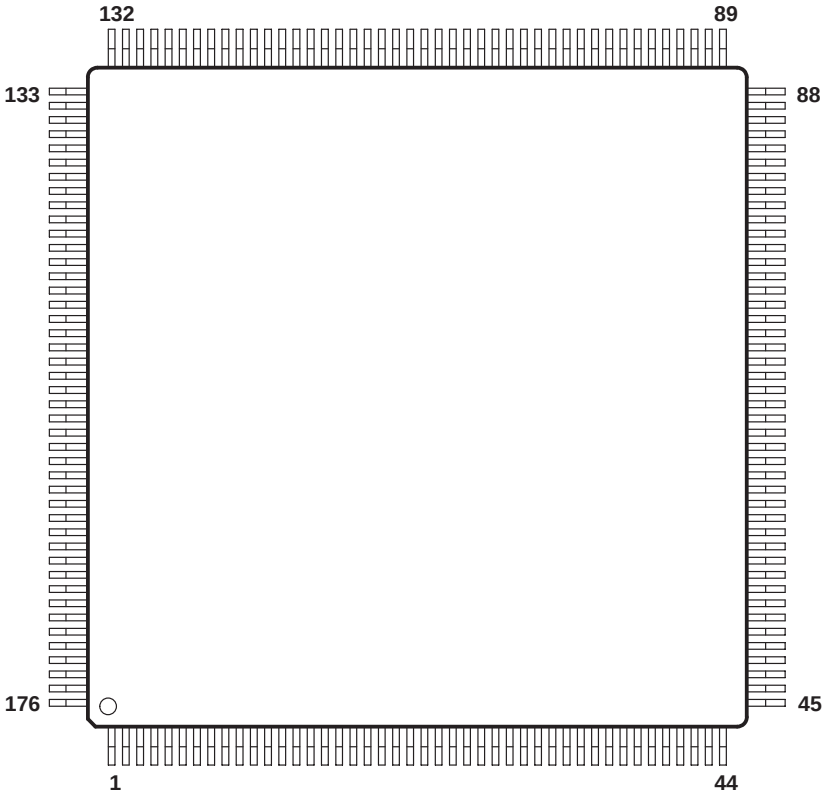


Figure 2−2. 176-Pin PGF Low-Profile Quad Flatpack (Top View)

Table 2–2. Pin Assignments for TMS320VC5441PGF (176-Pin LQFP Package)†

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	HA[0]/HCNTL0	2	HA[1]/HCNTL1	3	HA[2]/A_HINT	4	HA[3]/B_HINT
5	HA[4]/C_HINT	6	V_{SS}	7	V_{SS}	8	B_RS
9	B_NMI	10	B_INT	11	CLKMD	12	TDI
13	TESTB	14	DV_{DD}	15	HAS	16	HCS
17	V_{SS}	18	V_{SSA}	19	CLKIN	20	HRDY
21	V_{CCA}	22	CV_{DD}	23	CV_{DD}	24	EMU0
25	BCLKR2	26	BCLKX2	27	V_{SS}	28	BFSR2
29	BFSX2	30	CLKOUT	31	DV_{DD}	32	BDR2
33	BDX2	34	V_{SS}	35	A_RS	36	A_NMI
37	A_INT	38	TDO	39	HA[5]/D_HINT	40	HA[6]
41	HA[7]	42	HA[8]	43	V_{SS}	44	HA[9]
45	A_BFSX0	46	DV_{DD}	47	A_GPIO1/A_BIO	48	A_BFSR0
49	A_GPIO3/A_TOUT	50	V_{SS}	51	A_GPIO0/A_XF	52	A_BDR0
53	CV_{DD}	54	A_BDX0	55	CV_{DD}	56	CV_{DD}
57	CV_{DD}	58	A_GPIO2/A_WTOUT	59	A_BCLKR0	60	A_BCLKX0
61	V_{SS}	62	HD[8]	63	HD[9]	64	DV_{DD}
65	DV_{DD}	66	HD[10]	67	HD[11]	68	HD[12]
69	HD[13]	70	V_{SS}	71	HD[14]	72	HD[15]
73	C_BCLKX0	74	CV_{DD}	75	CV_{DD}	76	CV_{DD}
77	C_BDR0	78	CV_{DD}	79	C_GPIO3/C_TOUT	80	C_BCLKR0
81	C_GPIO0/C_XF	82	V_{SS}	83	C_BDX0	84	C_GPIO1/C_BIO
85	C_GPIO2/C_WTOUT	86	DV_{DD}	87	DV_{DD}	88	C_BFSR0
89	C_BFSX0	90	HA[10]	91	HA[11]	92	HA[12]
93	HA[13]	94	V_{SS}	95	HA[14]	96	TESTC
97	C_INT	98	HDS1	99	C_RS	100	BDX1
101	BDR1	102	BCLKR1	103	DV_{DD}	104	BFSR1
105	BFSX1	106	V_{SS}	107	BCLKX1	108	HMODE
109	CV_{DD}	110	HR/W	111	RESET	112	C_NMI
113	HDS2	114	V_{SS}	115	HPI_SEL1	116	HPI_SEL2
117	EMU1/OFF	118	DV_{DD}	119	TCK	120	TMS
121	TRST	122	TESTD	123	D_INT	124	D_NMI
125	D_RS	126	V_{SS}	127	V_{SS}	128	HA[15]
129	HA[16]	130	HA[17]	131	HA[18]	132	D_BFSR0
133	D_BFSX0	134	DV_{DD}	135	DV_{DD}	136	D_GPIO2/D_WTOUT
137	D_BDX0	138	D_BCLKR0	139	V_{SS}	140	D_BCLKX0
141	D_GPIO0/D_XF	142	CV_{DD}	143	D_BDR0	144	CV_{DD}
145	CV_{DD}	146	CV_{DD}	147	D_GPIO1/D_BIO	148	D_GPIO3/D_TOUT
149	HD[0]	150	V_{SS}	151	HD[1]	152	HD[2]
153	DV_{DD}	154	HD[3]	155	HD[4]	156	HD[5]
157	HD[6]	158	V_{SS}	159	HD[7]	160	B_BCLKR0
161	B_BCLKX0	162	CV_{DD}	163	CV_{DD}	164	CV_{DD}
165	B_BDR0	166	CV_{DD}	167	B_BDX0	168	B_GPIO3/B_TOUT
169	B_GPIO0/B_XF	170	V_{SS}	171	B_BFSR0	172	B_GPIO2/B_WTOUT
173	B_GPIO1/B_BIO	174	DV_{DD}	175	DV_{DD}	176	B_BFSX0

† Cells highlighted in gray indicate pins that perform a multiplexed function.

2.4 Signal Descriptions

Table 2−3 lists all the signals, grouped by function. See Section 2.3 for the exact pin locations based on the package type. Pin functions highlighted in gray are secondary (multiplexed) functions.

Table 2−3. Signal Descriptions

NAME	TYPE†	DESCRIPTION
HOST-PORT INTERFACE SIGNALS		
HA18 (MSB) HA17 HA16 HA15 HA14 HA13 HA12 HA11 HA10 HA9 HA8 HA7 HA6 HA5 HA4 HA3 HA2 HA1 HA0 (LSB)	I‡	HPI address pins when HPI is in nonmultiplexed mode. HA18 is used to facilitate program (shared) memory and data (local) memory selection. The pins include bus holders to reduce power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external pullup resistors on unused pins. When the address bus is not being driven by the external host, the bus holders keep address pins at the last driven logic level. The address bus keepers are disabled at global reset or subsystem A reset, and can be enabled/disabled via the BHA bit of the BSCR register in subsystem A. **SECONDARY** D_HINT, C_HINT, B_HINT, A_HINT — O/Z§ HCNTL1, HCNTL0 — I
HD15 (MSB) HD14 HD13 HD12 HD11 HD10 HD9 HD8 HD7 HD6 HD5 HD4 HD3 HD2 HD1 HD0 (LSB)	I/O/Z‡§	Parallel bidirectional data bus. These pins are the HPI data bus. The pins include bus holders to reduce power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external pullup resistors on unused pins. When the data bus is not being driven by the 5441, the bus holders keep data pins at the last driven logic level. The data bus keepers are disabled at global reset or subsystem A reset, and can be enabled/disabled via the BHD bit of the BSCR register in subsystem A.

† I = Input, O = Output, S = Supply, Z = High Impedance
‡ This pin has an internal bus holder controlled by way of the BSCR register in TMS320C54x™ cLEAD core of DSP subsystem A.
§ This pin is placed in high-impedance when the EMU1/$\overline{OFF}$ pin operates as $\overline{OFF}$ and when EMU1/$\overline{OFF}$ = 0, this case is exclusively for testing and emulation purposes.
¶ This pin has an internal pullup resistor.
# These pins are Schmitt triggered inputs.
‖ This pin is used by Texas Instruments for device testing and should be left unconnected.
☆ This pin has an internal pulldown resistor.
□ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.
NOTE: Pins highlighted in grey indicate the multiplexed function of the pin.

Table 2−3. Signal Descriptions (Continued)

NAME	TYPE†	DESCRIPTION
HOST-PORT INTERFACE SIGNALS (CONTINUED)		
HMODE¶	I	HPI mode select. When this pin is low, it selects the HPI multiplexed address/data mode. The multiplexed address/data mode allows hosts with multiplexed address/data lines access to the HPI registers HPIA, HPIC, and HPID. Host-to-DSP and DSP-to-host interrupts are supported in this mode. When HMODE is high, it selects the HPI nonmultiplexed mode. HPI nonmultiplexed mode allows hosts with separate address/data buses to access the HPI address range by way of the 19-bit address bus and the HPI data (HPID) register via the 16-bit data bus. Host-to-DSP and DSP-to-host interrupts are not supported in this mode.
$\overline{\text{HAS}}$¶#	I	HPI address latch enable (ALE) or address strobe input. Hosts with multiplexed address and data pins require $\overline{\text{HAS}}$ to latch the address in the HPIA register. This signal is used only in HPI multiplexed address/data mode (HMODE = 0).
HRDY	O/Z§	HPI data ready output. The ready output informs the host when the HPI is ready for the next transfer. While driving, it is in output state and while not driving, it is in high-Z state.
HR/$\overline{\text{W}}$	I	HPI read/write strobe. This signal is used by the host to control the direction of an HPI transfer.
$\overline{\text{HDS1}}$¶# $\overline{\text{HDS2}}$¶#	I	HPI data strobes. Driven by the host read and write strobes to control HPI transfers.
$\overline{\text{HCS}}$¶#	I	HPI chip select. Must be active during HPI transfers and can remain active between concurrent transfers.
		PRIMARY
$\overline{\text{D\_HINT}}$ $\overline{\text{C\_HINT}}$ $\overline{\text{B\_HINT}}$ $\overline{\text{A\_HINT}}$	O/Z§	HA5 HA4 HA3 HA2 — I Host interrupt pins. HPI can interrupt the host by asserting this low. The host can clear this interrupt by writing a “1” to the $\overline{\text{HINT}}$ bit of the HPIC register. Only supported in HPI multiplexed address/data mode (HMODE pin low)
HCNTL1 HCNTL0	I	HA1 HA0 — I HPI control pins. These pins select a host access to the HPIA, HPIC, and HPID registers. Only supported in HPI multiplexed address/data mode (HMODE pin low)
HPI_SEL1 HPI_SEL2	I	Subsystem HPI module select
MULTICHANNEL BUFFERED SERIAL PORTS 0, 1, AND 2 SIGNALS		
A_BCLKR0# B_BCLKR0# C_BCLKR0# D_BCLKR0#	I/O/Z§	Receive clocks. x_BCLKR0 serve as the serial shift clocks for the buffered serial-port receiver. Input from an external clock source for clocking data into the McBSP. When not being used as clocks, these pins can be used as general-purpose I/Os by setting RIOEN = 1. x_BCLKR0 can be configured as outputs by way of the CLKRM bit in the PCR register.
A_BCLKX0# B_BCLKX0# C_BCLKX0# D_BCLKX0#	I/O/Z§	Transmit clocks. Clock signals used to clock data from the transmit register. These pins can also be configured as inputs by setting CLKXM = 0 in the PCR register. x_BCLKX0 can be sampled as inputs by way of the IN1 bit in the SPC register. When not being used as clocks, these pins can be used as general-purpose I/Os by setting XIOEN = 1.
A_BDR0 B_BDR0 C_BDR0 D_BDR0	I	Buffered serial data receive (input) pins. When not being used as data-receive pins, these pins can be used as general-purpose I/Os by setting RIOEN = 1.

† I = Input, O = Output, S = Supply, Z = High Impedance
‡ This pin has an internal bus holder controlled by way of the BSCR register in TMS320C54x™ cLEAD core of DSP subsystem A.
§ This pin is placed in high-impedance when the EMU1/$\overline{\text{OFF}}$ pin operates as $\overline{\text{OFF}}$ and when EMU1/$\overline{\text{OFF}}$ = 0, this case is exclusively for testing and emulation purposes.
¶ This pin has an internal pullup resistor.
# These pins are Schmitt triggered inputs.
‖ This pin is used by Texas Instruments for device testing and should be left unconnected.
☆ This pin has an internal pulldown resistor.
□ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.
NOTE: Pins highlighted in grey indicate the multiplexed function of the pin.

Table 2−3. Signal Descriptions (Continued)

NAME	TYPE†	DESCRIPTION
MULTICHANNEL BUFFERED SERIAL PORTS 0, 1, AND 2 SIGNALS (CONTINUED)		
A_BDX0 B_BDX0 C_BDX0 D_BDX0	O/Z§	Buffered serial-port transmit (output) pins. When not being used as data-transmit pins, x_BDX0 can be used as general-purpose I/Os by setting XIOEN = 1.
A_BFSR0 B_BFSR0 C_BFSR0 D_BFSR0	I/O/Z§	Frame synchronization pins for buffered serial-port input data. The x_BFSR0 pulse initiates the receive-data process over x_BDR0. When not being used as data-receive synchronization pins, these pins can be used as general-purpose I/Os by setting RIOEN = 1.
A_BFSX0 B_BFSX0 C_BFSX0 D_BFSX0	I/O/Z§	Buffered serial-port frame synchronization pins for transmitting data. The x_BFSX0 pulse initiates the transmit-data process over the x_BDX0 pin. If $\overline{x\_RS}$ is asserted when x_BFSX0 is configured as output, then x_BFSX0 is turned into input mode by the reset operation. When not being used as data-transmit synchronization pins, these pins can be used as general-purpose I/Os by setting XIOEN = 1.
BCLKR1#	I	Receive clock, multiplexed McBSP1
BCLKX1#		Transmit clock, multiplexed McBSP1
BDR1		Receive data, multiplexed McBSP1
BDX1	O/Z§	Transmit data, multiplexed McBSP1
BFSR1	I	Receive frame sync, multiplexed McBSP1
BFSX1		Transmit frame sync, multiplexed McBSP1
BCLKR2#	I	Receive clock, multiplexed McBSP2
BCLKX2#		Transmit clock, multiplexed McBSP2
BDR2		Receive data, multiplexed McBSP2
BDX2	O/Z§	Transmit data, multiplexed McBSP2
BFSR2	I	Receive frame sync, multiplexed McBSP2
BFSX2		Transmit frame sync, multiplexed McBSP2
CLOCKING SIGNALS		
CLKOUT	O/Z§	Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the falling edges of this signal. The CLKOUT pin can be turned off by writing a “1” to the CLKOUT bit of the PMST register. Multiplexed as shown below based on the selection bits in the GPIO register
CLKIN#	I	Input clock to the device. CLKIN connects to a PLL.
CLKMD#	I	Clock mode configuration pin at reset. When CLKMD = 0, bypasses PLL; when CLKMD = 1, CLKINx2

	GPIO[7]	GPIO[6]	
A_CLKOUT	0	0	(default)
B_CLKOUT‖	0	1	
C_CLKOUT‖	1	0	
D_CLKOUT‖	1	1	

† I = Input, O = Output, S = Supply, Z = High Impedance
‡ This pin has an internal bus holder controlled by way of the BSCR register in TMS320C54x™ cLEAD core of DSP subsystem A.
§ This pin is placed in high-impedance when the EMU1/$\overline{OFF}$ pin operates as $\overline{OFF}$ and when EMU1/$\overline{OFF}$ = 0, this case is exclusively for testing and emulation purposes.
¶ This pin has an internal pullup resistor.
# These pins are Schmitt triggered inputs.
‖ This pin is used by Texas Instruments for device testing and should be left unconnected.
☆ This pin has an internal pulldown resistor.
□ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{TRST}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.
NOTE: Pins highlighted in grey indicate the multiplexed function of the pin.

Table 2−3. Signal Descriptions (Continued)

NAME	TYPE†	DESCRIPTION		
GENERAL-PURPOSE I/O PINS				
A_GPIO0/ A_XF	I/O/Z§	Subsystem A GPIO0/ Subsystem A external flag output	These pins act according to the general-purpose I/O register. The x_XF bit must be set to “1” to drive the x_XF output on the pin. If x_XF=0, then these pins are general-purpose I/Os.	General-purpose I/O pins (software-programmable I/O signal). Values can be latched (output) by writing into the GPIO register. The states of GPIO pins (inputs) can be determined by reading the GPIO register. The GPIO direction is also programmable by way of the DIRn field in the register.
B_GPIO0/ B_XF		Subsystem B GPIO0/ Subsystem B external flag output		
C_GPIO0/ C_XF		Subsystem C GPIO0/ Subsystem C external flag output		
D_GPIO0/ D_XF		Subsystem D GPIO0/ Subsystem D external flag output		
A_GPIO1/ A_BIO	I/O/Z§	Subsystem A GPIO1/ Subsystem A branch control input	These pins act according to the general-purpose I/O register. The x_BIO bit must be set to “1” to drive the x_BIO input into the device. If x_BIO=0, then these pins are general-purpose I/Os.	
B_GPIO1/ B_BIO		Subsystem B GPIO1/ Subsystem B branch control input		
C_GPIO1/ C_BIO		Subsystem C GPIO1/ Subsystem C branch control input		
D_GPIO1/ D_BIO		Subsystem D GPIO1/ Subsystem D branch control input		
A_GPIO2/ A_WTOUT	I/O/Z§	Subsystem A GPIO2/ Subsystem A watchdog timer output	The watchdog enable (WDEN) bit in the watchdog timer register (WDTSCR) is used to multiplex the watchdog timer output and GPIO2. If WDEN=0, then these pins are general-purpose I/Os.	
B_GPIO2/ B_WTOUT		Subsystem B GPIO2/ Subsystem B watchdog timer output		
C_GPIO2/ C_WTOUT		Subsystem C GPIO2/ Subsystem C watchdog timer output		
D_GPIO2/ D_WTOUT		Subsystem D GPIO2/ Subsystem D watchdog timer output		
A_GPIO3/ A_TOUT	I/O/Z§	Subsystem A GPIO3/ Subsystem A timer output	These pins act according to the general-purpose I/O register. The X_TOUT bit must be set to “1” to drive the timer output on the pin. If X_TOUT=0, then these pins are general-purpose I/Os.	
B_GPIO3/ B_TOUT		Subsystem B GPIO3/ Subsystem B timer output		
C_GPIO3/ C_TOUT		Subsystem C GPIO3/ Subsystem C timer output		
D_GPIO3/ D_TOUT		Subsystem D GPIO3/ Subsystem D timer output		

† I = Input, O = Output, S = Supply, Z = High Impedance
‡ This pin has an internal bus holder controlled by way of the BSCR register in TMS320C54x™ cLEAD core of DSP subsystem A.
§ This pin is placed in high-impedance when the EMU1/$\overline{\text{OFF}}$ pin operates as $\overline{\text{OFF}}$ and when EMU1/$\overline{\text{OFF}}$ = 0, this case is exclusively for testing and emulation purposes.
¶ This pin has an internal pullup resistor.
# These pins are Schmitt triggered inputs.
‖ This pin is used by Texas Instruments for device testing and should be left unconnected.
☆ This pin has an internal pulldown resistor.
□ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.
NOTE: Pins highlighted in grey indicate the multiplexed function of the pin.

Table 2−3. Signal Descriptions (Continued)

NAME	TYPE†	DESCRIPTION
INITIALIZATION, INTERRUPT, AND RESET OPERATIONS		
A_INT¶# B_INT¶# C_INT¶# D_INT¶#	I	External user interrupts. A_INT−D_INT are prioritized and are maskable by the interrupt mask register (IMR) and the interrupt mode bit. The status of these pins can be polled and reset by way of the interrupt flag register (IFR).
A_NMI¶# B_NMI¶# C_NMI¶# D_NMI¶#	I	Nonmaskable interrupts. x_NMI is an external interrupt that cannot be masked by way of the INTM bit or the IMR. When x_NMI is activated, the processor traps to the appropriate vector location.
A_RS# B_RS# C_RS# D_RS#	I	Reset. x_RS causes the digital signal processor (DSP) to terminate execution and causes a reinitialization of the CPU and peripherals. When x_RS is brought to a high level, execution begins at location 0FF80h of program memory. x_RS affects various registers and status bits.
RESET#	I	Global/HPI reset. This signal resets the four subsystems and the HPI.
SUPPLY PINS		
V_{CCA}	S	Dedicated power supply that powers the PLL. V_{DD} = 1.6 V
CV_{DD}		Dedicated power supply that powers the core CPUs. CV_{DD} = 1.6 V
DV_{DD}		Dedicated power supply that powers the I/O pins. DV_{DD} = 3.3 V
V_{SS}		Digital ground. Dedicated ground plane for the device.
V_{SSA}		Analog ground. Dedicated ground for the PLL. V_{SSA} can be connected to V_{SS} if digital and analog grounds are not separated.
EMULATION/TEST PINS		
TESTB‖ TESTC‖ TESTD‖		No connection
TCK¶#	I	Standard test clock. This is normally a free-running clock signal with a 50% duty cycle. Changes on the test access port (TAP) input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test-data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK.
TDI¶	I	Test data input. Pin with an internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
TDO	O/Z§	Test data pin. The contents of the selected register is shifted out of TDO on the falling edge of TCK. TDO is in high-impedance state except when the scanning of data is in progress.
TMS¶	I	Test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK.
TRST☆□	I	IEEE standard 1149.1 test reset. TRST, when high, gives the IEEE standard 1149.1 scan system control of the operations of the device. If TRST is driven low, the device operates in its functional mode, and the IEEE standard 1149.1 signals are ignored. Pin with internal pulldown device.
EMU0	I/O/Z	Emulator interrupt 0 pin. When TRST is driven low, EMU0 must be high for the activation of the EMU1/OFF condition. When TRST is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as I/O.

† I = Input, O = Output, S = Supply, Z = High Impedance
‡ This pin has an internal bus holder controlled by way of the BSCR register in TMS320C54x™ cLEAD core of DSP subsystem A.
§ This pin is placed in high-impedance when the EMU1/OFF pin operates as OFF and when EMU1/OFF = 0, this case is exclusively for testing and emulation purposes.
¶ This pin has an internal pullup resistor.
# These pins are Schmitt triggered inputs.
‖ This pin is used by Texas Instruments for device testing and should be left unconnected.
☆ This pin has an internal pulldown resistor.
□ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the TRST pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.
NOTE: Pins highlighted in grey indicate the multiplexed function of the pin.

Table 2−3. Signal Descriptions (Continued)

NAME	TYPE†	DESCRIPTION
EMULATION/TEST PINS (CONTINUED)		
EMU1/$\overline{\text{OFF}}$	I/O/Z	Emulator interrupt 1 pin. When $\overline{\text{TRST}}$ is driven high, EMU1/$\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as I/O. When $\overline{\text{TRST}}$ transitions from high to low, then EMU1 operates as $\overline{\text{OFF}}$. EMU/$\overline{\text{OFF}}$ = 0 puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (and not for multiprocessing applications). Therefore, for the $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}}$ = 0, EMU0 = 1, EMU1 = 0

† I = Input, O = Output, S = Supply, Z = High Impedance
‡ This pin has an internal bus holder controlled by way of the BSCR register in TMS320C54x™ cLEAD core of DSP subsystem A.
§ This pin is placed in high-impedance when the EMU1/$\overline{\text{OFF}}$ pin operates as $\overline{\text{OFF}}$ and when EMU1/$\overline{\text{OFF}}$ = 0, this case is exclusively for testing and emulation purposes.
¶ This pin has an internal pullup resistor.
# These pins are Schmitt triggered inputs.
‖ This pin is used by Texas Instruments for device testing and should be left unconnected.
☆ This pin has an internal pulldown resistor.
□ Although this pin includes an internal pulldown resistor, a 470-Ω external pulldown is required. If the $\overline{\text{TRST}}$ pin is connected to multiple DSPs, a buffer is recommended to ensure the V_{IL} and V_{IH} specifications are met.
NOTE: Pins highlighted in grey indicate the multiplexed function of the pin.

3 Functional Overview

The functional overview in this section is based on the overall system block diagram in Figure 3−1 and the typical subsystem block diagram in Figure 3−2.

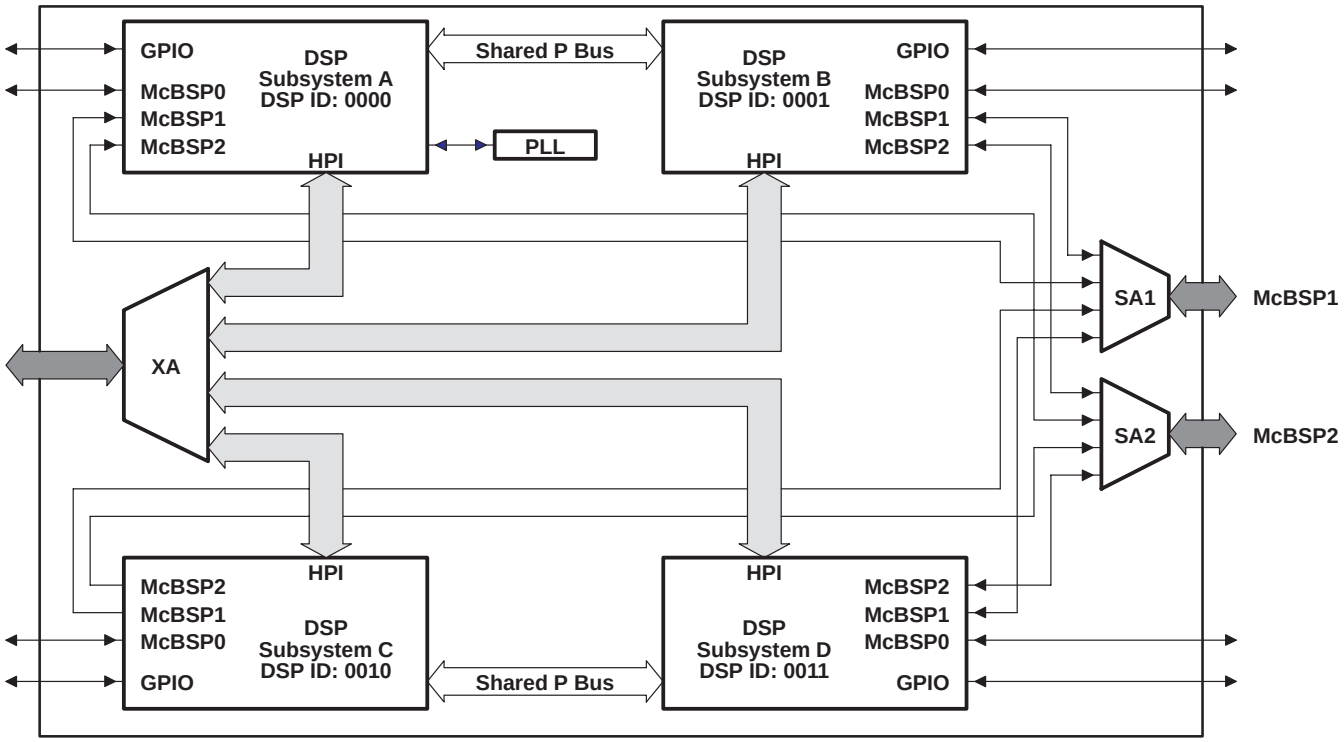


Figure 3−1. Overall Functional Block Diagram

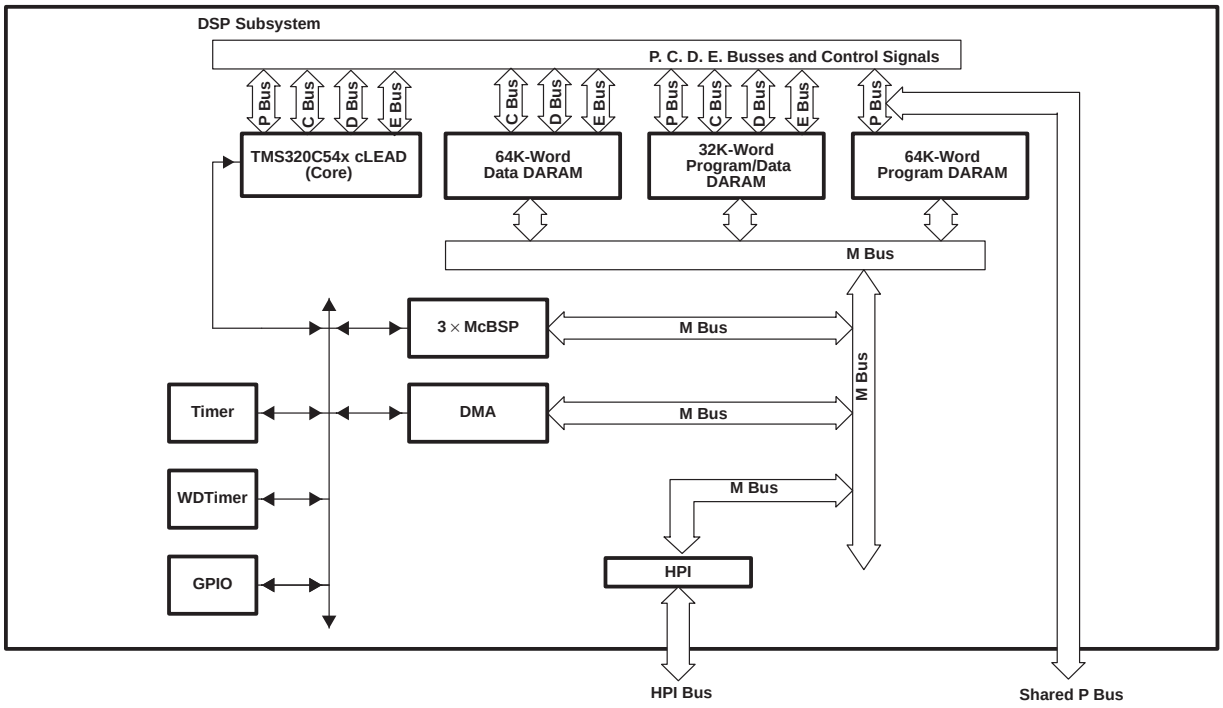


Figure 3−2. Typical Subsystem Functional Block Diagram

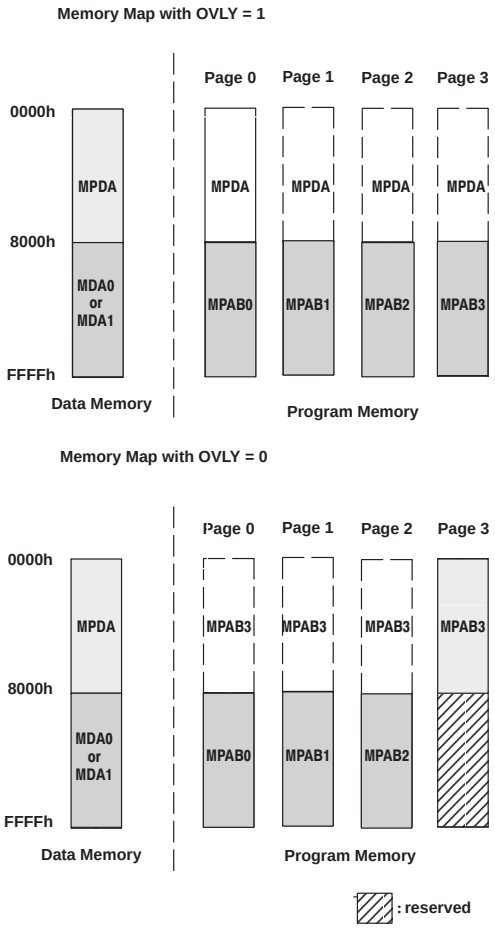
3.1 Memory

Each 5441 DSP subsystem maintains the peripheral register memory map and interrupt location/priorities of the standard 5421. Each individual subsystem CPU memory map is illustrated in Figure 3−3 through Figure 3−6.

The arbitration and access for local program/data memory and local data memory is based on a 16K-word block size. The arbitration and access for all the shared memory is based on a 32K-word block size.

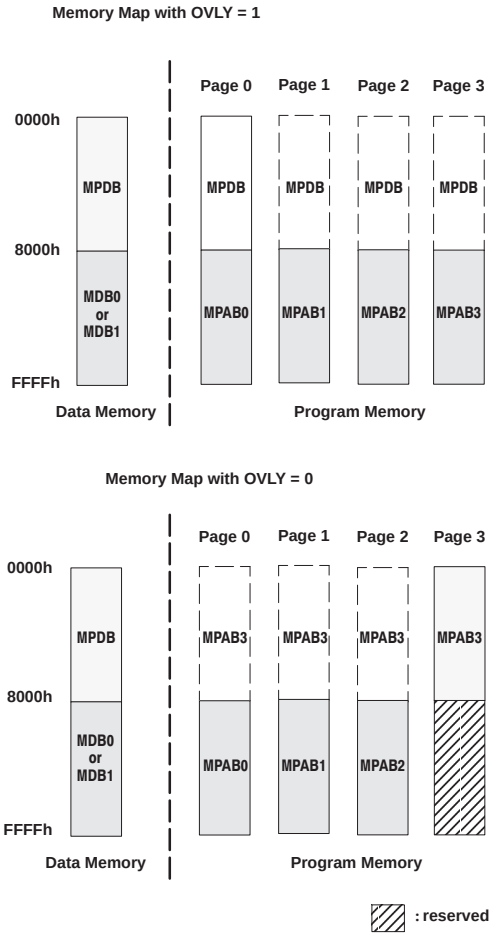
3.1.1 Memory Maps

Figure 3−3 through Figure 3−6 illustrate the CPU memory maps for subsystem A through subsystem D. Figure 3−7 provides a detailed memory map of the local data memory relative to CPU subsystems A, B, C, and D.



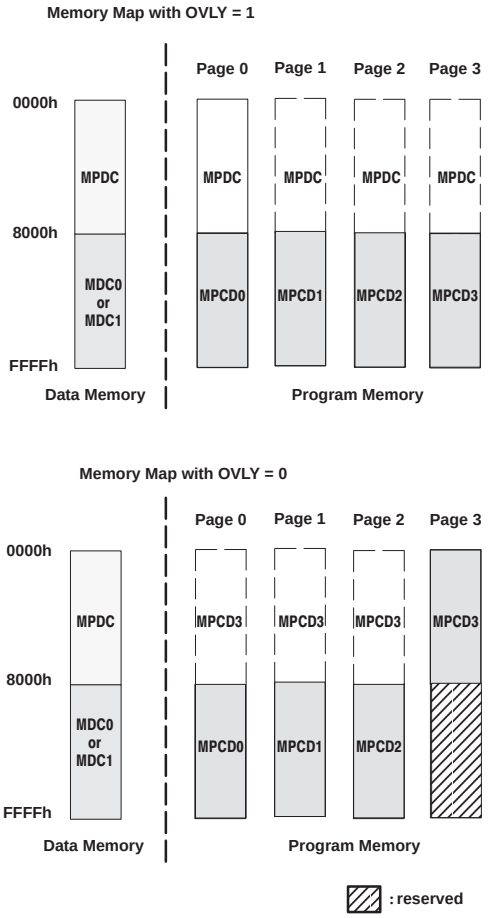
NOTES: A. MPDA: local program/data memory in subsystem A
B. MDA: local data memory in subsystem A. MDA is controlled by the data memory map register (DMMR).
DMMR=0, MDA0 is mapped in 8000h − FFFFh.
DMMR=1, MDA1 is mapped in 8000h − FFFFh.
C. MPAB: shared program memory in subsystems A and B

Figure 3−3. Subsystem A CPU Memory Map



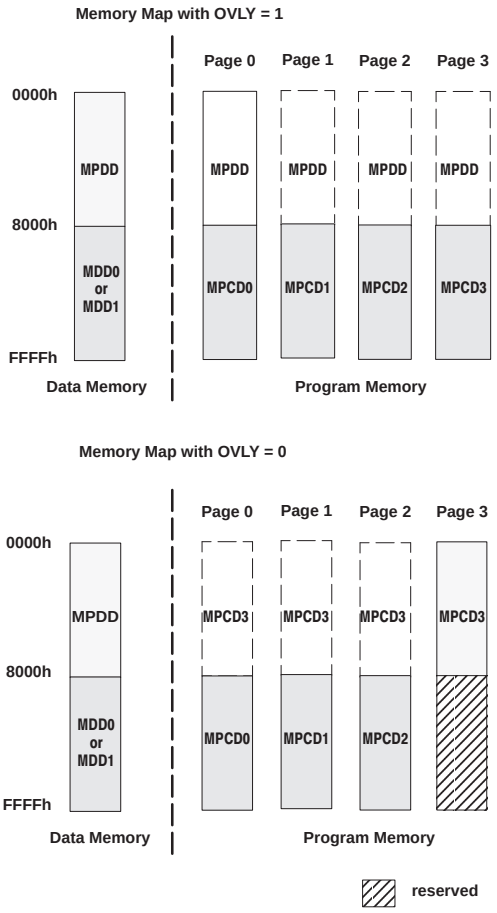
NOTES: A. MPDB: local program/data memory in subsystem B
B. MDB: local data memory in subsystem B. MDB is controlled by the data memory map register (DMMR).
DMMR=0, MDB0 is mapped in 8000h − FFFFh.
DMMR=1, MDB1 is mapped in 8000h − FFFFh.
C. MPAB: shared program memory in subsystems A and B

Figure 3−4. Subsystem B CPU Memory Map



NOTES: A. MPDC: local program/data memory in subsystem C
B. MDC: local data memory in subsystem C. MDC is controlled by the data memory map register (DMMR).
DMMR=0, MDC0 is mapped in 8000h − FFFFh.
DMMR=1, MDC1 is mapped in 8000h − FFFFh.
C. MPCD: shared program memory in subsystems C and D

Figure 3−5. Subsystem C CPU Memory Map



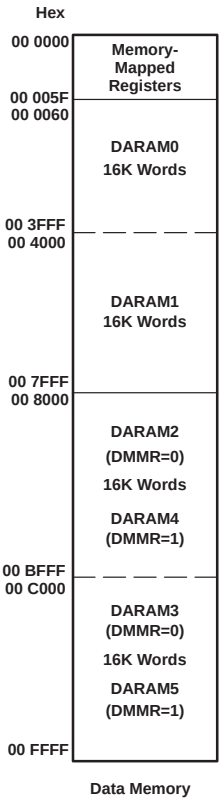
NOTES: A. MPDD: local program/data memory in subsystem D
B. MDD: local data memory in subsystem D. MDD is controlled by the data memory map register (DMMR).
DMMR=0, MDD0 is mapped in 8000h − FFFFh.
DMMR=1, MDD1 is mapped in 8000h − FFFFh.
C. MPCD: shared program memory in subsystems C and D

Figure 3−6. Subsystem D CPU Memory Map

Figure 3−7 shows the CPU data memory map. The lower 32K-word data memory location in all pages is the overlay area. Program memory has overlay area over the lower 32K words on all pages as well.

The overlay areas refer to:

1. When OVLY = 1, the lower 32K words of data space are mapped to the lower 32K words of all program pages in the memory map.
2. When OVLY = 0, the lower 32K words of data space are mapped only to the lower 32K words of data space and the lower 32K words of program page 3 are mapped to the lower 32K words of all program pages.



NOTE: The upper part of data memory is controlled by the Data Memory Map Register (DMMR).
1. DMMR=0, DARAM2 and DARAM3 are mapped in 8000h − FFFFh.
2. DMMR=1, DARAM4 and DARAM5 are mapped in 8000h − FFFFh.

Figure 3−7. Detailed Memory Map of Local Data Memory Relative to CPU Subsystems A, B, C, and D

3.1.2 On-Chip Dual-Access RAM (DARAM)

Each 5441 subsystem has 96K 16-bit words of on-chip DARAM (six blocks of 16K words). Each of these DARAM blocks can be accessed twice per machine cycle. This memory is intended primarily to store data values; however, it can be used to store program as well. At reset, the DARAM is mapped into data memory space (OVLY=0). The lower part of DARAM (0000h−8000h) can be mapped into program/data memory space by setting the OVLY bit in the processor-mode status (PMST) register of the TMS320C54x™ cLEAD CPU in each DSP subsystem.

3.1.3 On-Chip Two-Way Shared RAM

There are 128K 16-bit words of on-chip RAM (four blocks of 32K words) that are shared between subsystems A and B. There are 128K 16-bit words of on-chip RAM (four blocks of 32K words) that are shared between subsystems C and D. This memory is intended to store program only. Both subsystems are able to make one instruction fetch from any location in the two-way shared memory each cycle simultaneously. No subsystem CPU can write to the shared memory as only the DMA can write to shared memory.

If any of the CPU program fetches are requested at the same time as an M-bus transfer request, the CPU is stalled until all M bus transfers are completed. In other words, any read or write requested by the M bus (driven by DMA controller or HPI) has priority over the CPUs' (A, B, C, and D) program fetches. The M-bus reads or writes always take two cycles to complete.

3.1.4 Extended Data Memory

The data memory space of each 5441 subsystem addresses 128K 16-bit words. There are two pages of data memory location with each page consisting of 64K words. The 5441 device uses a data memory map register (DMMR) to facilitate extended data memory access. The DMMR is a peripheral memory-mapped register. The contents of the DMMR register, once being written with an extended data number by the DSP CPU, will be associated with the address decoding for all the data memory CPU accesses.

3.1.5 Extended Program Memory

The 5441 device uses a paged extended memory scheme in program space to allow access to 256K 16-bit words. This extended program memory (each subsystem) is organized into four pages (0−3), pages 0−3 are two-way shared memory. Each page is 64K words in length. The program counter extension register (XPC) defines the program page selection. To implement the extended program memory scheme, the 5441 device includes the following feature:

- Two C54x™ instructions allow each subsystem CPU access to the on-chip program memory.
  - READA − Read program memory addressed by accumulator A and store in data memory
  - WRITA − Write data to program memory addressed by accumulator A
    (Writes not allowed for CPUs to shared program memory)

3.1.6 Program Memory

The program memory is accessible on multiple pages, depending on the XPC value. Within these pages, memory is accessible depending on the address range.

- Access in the lower 32K words of each page is dependent on the state of OVLY.
  - OVLY = 0 − Program memory is accessed from program memory page 3 for all values of XPC.
  - OVLY = 1 − Program memory is accessed from local data/program DARAM for all values of XPC.
- Access in the upper 32K words of each page is dependent on the state of OVLY.
  - OVLY = 0 − All pages of program memory except page 3 (which is reserved) are accessible for all values of XPC.
  - OVLY = 1 − All pages of program memory are accessible for all values of XPC.

3.1.7 Data Memory

Accesses on extended data spaces are dependent on the value of the data memory map register (DMMR). Within the page, memory is accessible depending on the address range.

- Access in the lower 32K words
  - Data memory is accessed from local data/program DARAM for all values of DMMR.
- Access in the upper 32K words
  - Which data memory block is accessed depends on the value of DMMR.
  - There are four 16K-word DARAM blocks for the upper addresses (8000h − FFFFh)
    DMMR=0: DARAM2 and DARAM3 are mapped to the upper addresses
    DMMR=1: DARAM4 and DARAM5 are mapped to the upper addresses

3.1.8 I/O Memory

The 5441 does not support I/O memory accesses.

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3.1.9 Multicore Reset Signals

The 5441 device includes five reset signals: $\overline{\text{A\_RS}}$, $\overline{\text{B\_RS}}$, $\overline{\text{C\_RS}}$, $\overline{\text{D\_RS}}$, and $\overline{\text{RESET}}$. The $\overline{\text{A\_RS}}$, $\overline{\text{B\_RS}}$, $\overline{\text{C\_RS}}$, and $\overline{\text{D\_RS}}$ local reset signals function as the CPU reset signal for subsystem A, B, C, and D, respectively. The $\overline{\text{RESET}}$ services as a global reset for the whole device.

The global reset ($\overline{\text{RESET}}$) is a superset of local resets $\overline{\text{A\_RS}}$, $\overline{\text{B\_RS}}$, $\overline{\text{C\_RS}}$, and $\overline{\text{D\_RS}}$. The assertion of $\overline{\text{RESET}}$ triggers all the local resets; however, none of the local resets triggers the global reset. The local reset signals reset the state of the CPU registers and CPU memory-mapped peripheral registers, and upon release, initiate the reset function. The global reset, $\overline{\text{RESET}}$, resets the on-chip PLL and clears the watchdog timer flag (WDFLAG) bit. The local reset signals are not able to reset the PLL or clear the WDFLAG.

The global reset ($\overline{\text{RESET}}$) and local resets ($\overline{\text{x\_RS}}$) clears the program counter extension register (XPC) to zero while the $\overline{\text{RESET}}$ instruction does not affect the XPC.

3.1.10 Device Bootload

The 5441 device supports an HPI boot sequence, which is used to download code while the DSP is in reset. The external master holds the device in reset while it loads code to the on-chip memory of each subsystem, subsystem selection is made by HPI_SEL1 and HPI_SEL2 signals. The host can release the 5441 from reset by using either of the following methods.

- If the $\overline{\text{x\_RS}}$ (x = A, B, C, or D for subsystem A, B, C, or D, respectively) pins are held low while $\overline{\text{RESET}}$ transitions from low to high, the reset of each subsystem will be controlled by the $\overline{\text{x\_RS}}$ pins. When the host has finished downloading code, it can drive $\overline{\text{x\_RS}}$ high to release the cores from reset.
- If the $\overline{\text{x\_RS}}$ pins are held high while $\overline{\text{RESET}}$ transitions from low to high, the subsystems will stay in reset until an HPI data write to address 0x2F occurs. This means the host can download code to subsystem x and then release core x from reset by writing any data to core x's address 0x2F via the HPI. The host can then repeat the sequence for other cores. This mode allows the host to control 5441 reset without additional hardware.

3.2 On-Chip Peripherals

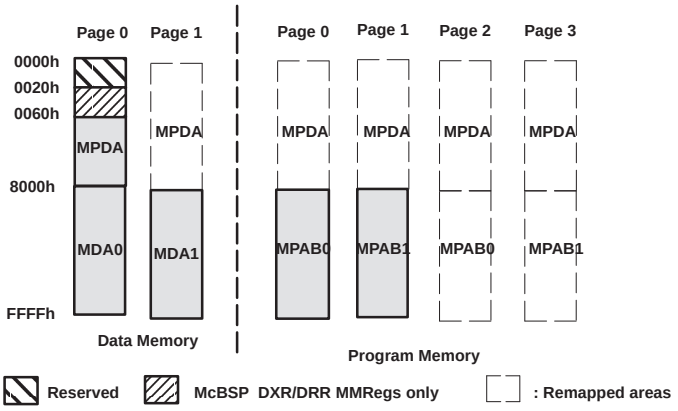
All the C54x™ devices have the same CPU structure; however, they have different on-chip peripherals connected to their CPUs. The on-chip peripheral options provided are:

- DMA controller
- 16-bit host-port interface I/O ports
- Multichannel buffered serial ports (McBSPs)
- A hardware timer
- A hardware watchdog timer
- A software-programmable clock generator using a phase-locked loop (PLL)
- General-purpose I/O

3.2.1 Direct Memory Access (DMA) Controller

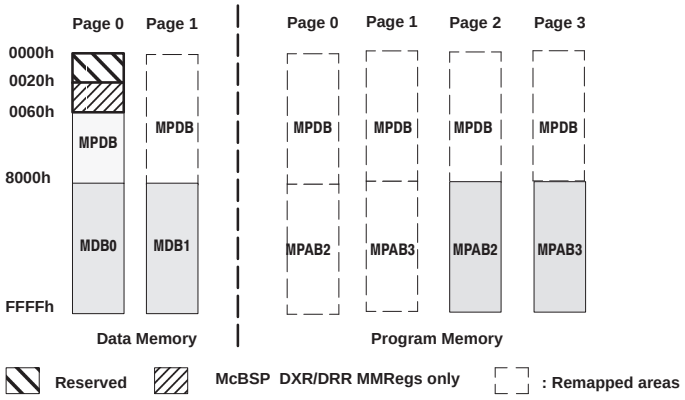
The 5441 includes four 6-channel direct memory access (DMA) controllers for performing data transfers independent of the CPU, one controller for each subsystem. The primary function of the 5441 DMA controller is to provide code overlays and to manage data transfers between on-chip memory, the peripherals, and off-chip host.

In the background of CPU operation, the 5441 DMA allows movement of data between internal program/data memory and internal peripherals, such as the McBSPs and the HPI. Each subsystem has its own independent DMA with six programmable channels, which allows for six different contexts for DMA operation. The HPI has a dedicated auxiliary DMA channel. The remapped areas represent address aliasing for DMA accesses within each subsystem. Figure 3−8 through Figure 3−11 illustrate the local DMA memory map of each subsystem.



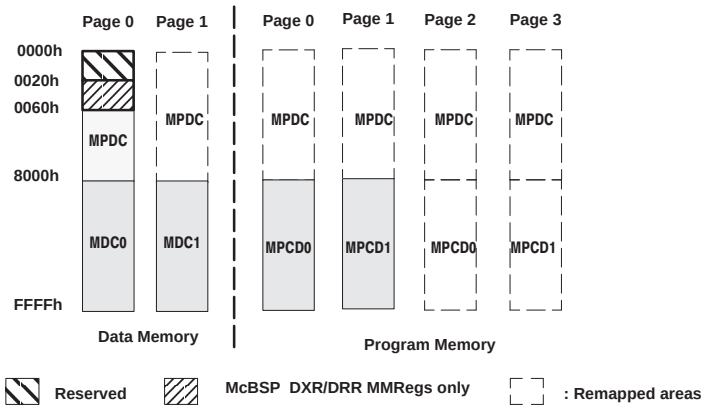
NOTES: A. MPDA: local program/data memory in subsystem A
B. MDA: local data memory in subsystem A
C. MPAB: two-way shared program memory in subsystems A and B

Figure 3−8. Subsystem A Local DMA Memory Map



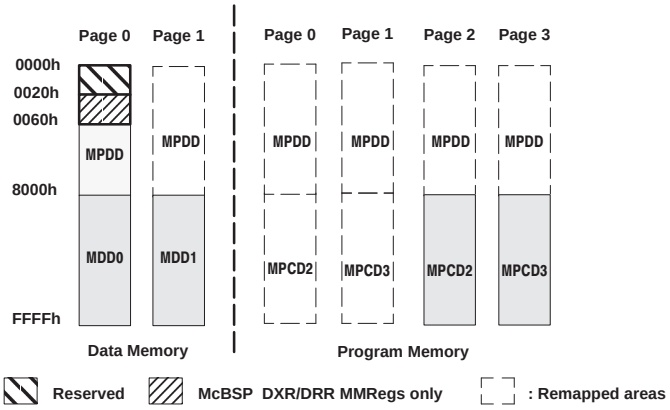
NOTES: A. MPDB: local program/data memory in subsystem B
B. MDB: local data memory in subsystem B
C. MPAB: two-way shared program memory in subsystems A and B

Figure 3−9. Subsystem B Local DMA Memory Map



NOTES: A. MPDC: local program/data memory in subsystem C
B. MDC: local data memory in subsystem C
C. MPCD: two-way shared program memory in subsystems C and D

Figure 3−10. Subsystem C Local DMA Memory Map



NOTES: A. MPDD: local program/data memory in subsystem D
B. MDD: local data memory in subsystem D
C. MPCD: two-way shared program memory in subsystems C and D

Figure 3−11. Subsystem D Local DMA Memory Map

3.2.1.1 DMA Controller Features

The 5441 DMA has the following features:

- The DMA operates independently of the CPU.
- The DMA has six channels. The DMA can keep track of the contexts of six independent block transfers.
- The DMA has higher priority than the CPU.
- Each channel has independently programmable priority.
- Each channel's source and destination address registers include configurable indexing modes. The address can be held constant, postincremented, postdecremented, or adjusted by a programmable value.
- Each read or write transfer can be initialized by selected events.
- The DMA supports single-word (16-bit) and double-word (32-bit) transfers.
- Each DMA channel has independent reload registers.
- Each DMA channel has independent extended source/destination data page registers.
- The DMA does not support I/O memory access.

A 16-bit DMA transfer requires four CPU clock cycles to complete—two cycles for reads and two cycles for writes. Since the DMA controller shares the DMA bus with the HPI module, the DMA access rate is reduced when the HPI is active.

3.2.1.2 DMA Reload Registers

Each DMA channel has its own reload registers which are utilized when autoinitialization is enabled for the current DMA channel. The reload registers include:

- Source address reload register (DMGSAn)
- Destination address reload register (DMGDAn)
- Element count reload register (DMGCRn)
- Frame count reload register (DMGFRn)

The "n" in the register names refers to DMA channel number: 0, 1, 2, 3, 4, and 5.

In the DMPREC register, bit 14 (IAUTO) is used to enable individual reload register for each channel. If that bit is not set, the channel 0 reload register will be loaded to all chanels (this is backward compatible).

3.2.1.3 Extended Source/Destination Data Page Registers (DMSRCDPn/DMDSTDPn)

The DMA controller has the ability to perform transfers to and from the extended data memory space. The DMA extended source data page register and extended destination data page register service this purpose and only the least significant seven bits are used to designate the extended data memory page. Each of the DMA channels will have one set of these registers for extended data memory page (other than page 0) access. Data memory space transfers cannot cross 64K page boundaries. If a data page boundary is crossed during a transfer, the next transfer will wrap on to the same page.

For detailed information on DMA registers, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

3.2.1.4 DMA Controller Synchronization Events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMA channel x sync select and frame count (DMSFCx) register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in Table 3−1.

Table 3−1. DMA Synchronization Events

DSYN VALUE	DMA SYNCHRONIZATION EVENT
0000b	No synchronization used
0001b	McBSP0 Receive Event
0010b	McBSP0 Transmit Event
0011b	McBSP2 Receive Event
0100b	McBSP2 Transmit Event
0101b	McBSP1 Receive Event
0110b	McBSP1 Transmit Event
0111b − 1111b	Reserved

3.2.1.5 DMA Channel Interrupt Selection

The DMA controller can generate a CPU interrupt for each of the six channels. However, channels 0, 1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 0 and 1 share an interrupt line with the receive and transmit portions of McBSP2 (IMR/IFR bits 6 and 7), and DMA channels 2 and 3 share an interrupt line with the receive and transmit portions of McBSP1 (IMR/IFR bits 10 and 11). When the 5441 is reset, the interrupts from these four DMA channels are deselected. The INTSEL bit field in the DMA channel priority and enable control (DMPREC) register can be used to select these interrupts, as shown in Table 3−2.

Table 3−2. DMA Channel Interrupt Selection

INTSEL Value	IMR/IFR[6]	IMR/IFR[7]	IMR/IFR[10]	IMR/IFR[11]
00b (reset)	BRINT2	BXINT2	BRINT1	BXINT1
01b	BRINT2	BXINT2	DMAC2	DMAC3
10b	DMAC0	DMAC1	DMAC2	DMAC3
11b	Reserved			

3.2.2 16-Bit Bidirectional Host-Port Interface (HPI16)

3.2.2.1 HPI16 Memory Map

The HPI16 is an enhanced 16-bit version of the C54x™ DSP 8-bit host-port interface (HPI). The HPI16 is designed to allow a 16-bit host to access the DSP on-chip memory, with the host acting as the master of the interface. Each HPI subsystem memory map is identical to its corresponding DMA memory map except the HPI memory map does not support accesses to any memory-mapped registers.

Some of the features of the HPI16 include:

- A 16-bit bidirectional data bus
- Multiple data strobes and control signals to allow glueless interfacing to a variety of hosts
- Multiplexed and nonmultiplexed address/data modes
- A 19-bit address bus used in nonmultiplexed mode to allow access to all on-chip (including extended address pages) memory
- A 19-bit address register used in multiplexed mode. Includes address autoincrement feature for faster accesses to sequential addresses
- Interface to on-chip DMA module to allow access to entire on-chip memory space
- HRDY signal to hold off host accesses due to DMA latency
- Control register available in multiplexed mode only. Accessible by either host or DSP to provide host/DSP interrupts, extended addressing, and data prefetch capability
- HPI_SEL1 and HPI_SEL2 pins are used to make selection among the four subsystem HPI modules.
- Both the HPI data bus and address bus have bus-holder features. The bus holders can be enabled/disabled by the CPUs.

3.2.2.2 HPI Multiplexed Mode

In *multiplexed* mode, HPI16 operation is very similar to that of the standard 8-bit HPI, which is available with other C54x™ DSP products. A host with a multiplexed address/data bus can access the HPI16 data register (HPID), address register (HPIA), or control register (HPIC) via the HD bidirectional data bus. The host initiates the access with the strobe signals ($\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, $\overline{\text{HCS}}$) and controls the type of access with the HCNTL, HR/$\overline{\text{W}}$, and $\overline{\text{HAS}}$ signals. The DSP can interrupt the host via the $\overline{\text{x\_HINT}}$ signal, and can stall host accesses via the HRDY signal. Bit 20 of the HPIA register is used to make selection between program (shared) memory and data (local) memory access. Table 3−3 shows the memory selection via HA[20].

Table 3−3. HPI Local/Shared Memory Selection Via HA[20]

HA[20]	Memory Type
0	Local (data)
1	Shared (program)

3.2.2.3 Host/DSP Interrupts

In *multiplexed* mode, the HPI16 offers the capability for the host and DSP to interrupt each other through the HPIC register.

For host-to-DSP interrupts, the host must write a “1” to the DSPINT bit of the HPIC register. This generates an interrupt to the DSP. This interrupt can also be used to wake the DSP from any of the IDLE 1,2, or 3 states. Note that the DSPINT bit is always read as “0” by both the host and DSP. The DSP cannot write to this bit (see Figure 3−12).

For DSP-to-host interrupts, the DSP must write a “1” to the $\overline{\text{HINT}}$ bit of the HPIC register to interrupt the host via the $\overline{\text{x\_HINT}}$ pin. The host acknowledges and clears this interrupt by also writing a “1” to the $\overline{\text{HINT}}$ bit of the HPIC register. Note that writing a “0” to the $\overline{\text{HINT}}$ bit by either host or DSP has no effect.

3.2.2.4 HPI Nonmultiplexed Mode

In *nonmultiplexed* mode, a host with separate address/data buses can access the HPI16 data register (HPID) via the 16-bit HD bidirectional data bus, and the address register (HPIA) via the 19-bit HA address bus. The HA[18] signal is used to make selection between program (shared) memory and data (local) memory access. Table 3−4 shows the memory selection via HA[18].

Table 3−4. HPI Local/Shared Memory Selection Via HA[18]

HA[18]	Memory Type
0	Local (data)
1	Shared (program)

The host initiates the access with the strobe signals ($\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, and $\overline{\text{HCS}}$) and controls the direction of the access with the HR/$\overline{\text{W}}$ signal. The HPI16 can stall host accesses via the HRDY signal. Note that the HPIC register is not available in *nonmultiplexed* mode since there are no HCNTL signals available. All host accesses initiate a DMA read or write access. Figure 3−12 shows a block diagram of the HPI16 in *nonmultiplexed* mode.

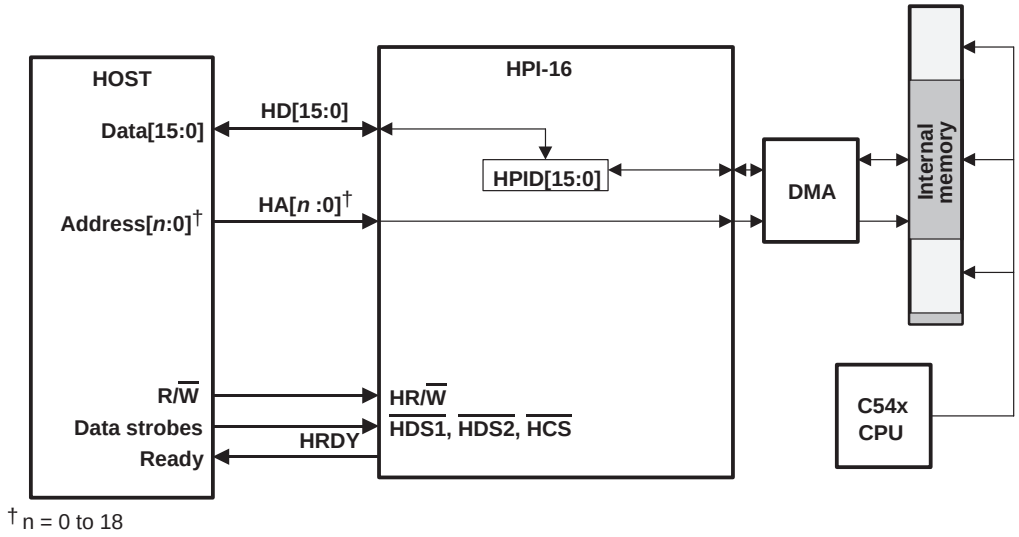


Figure 3−12. Interfacing to the HPI-16 in Non-Multiplexed Mode

3.2.2.5 HPI Bus Holder Control

Both the HPI data and address buses have bus holders. By default, the bus holders are disabled after global reset or subsystem A reset. The bus holders are configured via the BHD and BHA bits in the bank switching control register (BSCR) located at 29h in subsystem A. Figure 3−13 shows the BSCR bit layout for subsystem A and Table 3−5 describes the bit functions of BSCR.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													BHD	BHA	Reserved
						U							R/W+0	R/W+0	U

LEGEND: R = Read, W = Write, U = Undefined

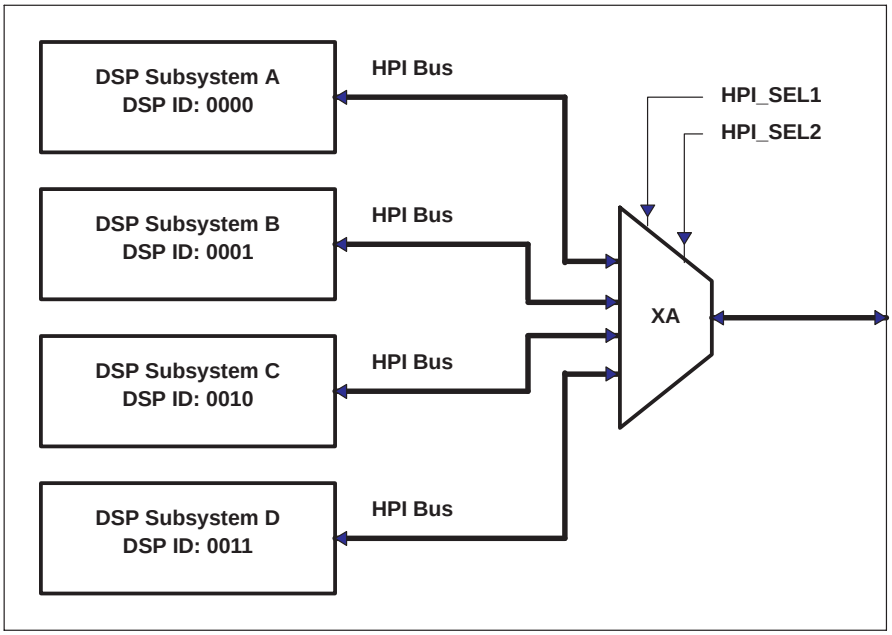
Figure 3−13. BSCR Register Bit Layout for Subsystem A

Table 3−5. BSCR Register Bit Functions for Subsystem A

BIT NO.	BIT NAME	FUNCTION
15−3	Reserved	These bits are reserved and are read as 0.
2	BHD	Data bus holder. BHD is cleared to 0 at reset. BHD = 0: The HPI data bus holder is disabled. BHD = 1: The HPI data bus holder is enabled.
1	BHA	Address bus holder. BHA is cleared to 0 at reset. BHA = 0: The HPI address bus holder is disabled. BHA = 1: The HPI address bus holder is enabled.
0	Reserved	This bit is reserved and is read as 0.

3.2.2.6 Other HPI16 System Considerations

- Operation During IDLE − The HPI16 can continue to operate during IDLE1 or IDLE2 by using special clock management logic that turns on relevant clocks to perform a synchronous memory access, and then turns the clocks back off to save power. The DSP CPU does not wake up from the IDLE mode during this process.
- Downloading Code During Reset − The HPI16 can download code while the DSP is in reset. The system provides a pin ($\overline{\text{RESET}}$) that provides a way to take the HPI16 module out of reset while leaving the DSP in reset.
- Emulation considerations − The HPI16 can continue operation even when the DSP CPU is halted due to debugger breakpoints or other emulation events.
- XA Multiplexer − XA multiplexer controls the HPI data traffic from each subsystem to the device boundary. The HPI module is the slave on the HPI bus. Figure 3−14 shows the 5441 block diagram with XA logic. The XA basic function includes:
  - Making the HPI bus available for the selected subsystem HPI module according to HPI selection pins HPI_SEL1/HPI_SEL2.
  - Granting HPI path to one of the subsystems at one time
- The HPI_SEL1 and HPI_SEL2 pins are used to select the HPI module among the four cores. The selection is indicated in Table 3−6.



NOTE: XA is the MUXing logic for HPI access.

Figure 3−14. XA Multiplexer for HPI Access

Table 3−6. HPI Module Selection

HPI_SEL2	HPI_SEL1	SELECTED HPI MODULE
0	0	Subsystem A
0	1	Subsystem B
1	0	Subsystem C
1	1	Subsystem D

3.2.3 Multichannel Buffered Serial Port (McBSP)

The 5441 device provides high-speed, full-duplex serial ports that allow direct interface to other C54x/LC54x devices, codecs, and other devices in a system. There are twelve multichannel buffered serial ports (McBSPs) on chip (three per subsystem).

The McBSP provides:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSP has the following capabilities:

- Direct interface to:
  - T1/E1 framers
  - MVIP switching-compatible and ST-BUS compliant devices
  - IOM-2 compliant device
  - AC97-compliant device
  - Serial peripheral interface (SPI)
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including: 8, 12, 16, 20, 24, or 32 bits
- µ-law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

3.2.3.1 McBSP Clock Source

The 5441 McBSPs allow either the receive clock pin (BCLKRn) or the transmit clock pin (BCLKXn) to be configured as the input clock to the sample rate generator. This enhancement is enabled through two register bits: bit 7 [the enhanced sample clock mode bit (SCLKME)] of the pin control register (PCR), and bit 13 [the McBSP sample rate generator clock mode bit (CLKSM)] of the sample rate generator register 2 (SRGR2). SCLKME is an addition to the PCR contained in the McBSPs on previous TMS320C5000™ DSP platform devices. The new bit layout of the PCR is shown in Figure 3−15. For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

15	14	13	12	11	10	9	8
Reserved		XIOEN	RIOEN	FSXM	FSRM	CLKXM	CLKRM
R,+0		RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0

7	6	5	4	3	2	1	0
SCLKME	CLKS_STAT	DX_STAT	DR_STAT	FSXP	FSRP	CLKXP	CLKRP
RW,+0	R,+0	R,+0	R,+0	RW,+0	RW,+0	RW,+0	RW,+0

LEGEND: R = Read, W = Write, +0 = Value at reset

Figure 3−15. Pin Control Register (PCR)

TMS320C5000 is a trademark of Texas Instruments.

The selection of the sample rate generator (SRG) clock input source is made by the combination of the CLKSM and SCLKME bit values as shown in Table 3−7.

Table 3−7. Sample Rate Generator Clock Source Selection

SCLKME	CLKSM	SRG Clock Source
0	0	Reserved
0	1	CPU clock
1	0	BCLKRn pin
1	1	BCLKXn pin

When either of the bidirectional pins, BCLKRn or BCLKXn, is configured as the clock input, its output buffer is automatically disabled. For example, with SCLKME = 1 and CLKSM = 0, the BCLKRn pin is configured as the SRG input. In this case, both the transmitter and receiver circuits can be synchronized to the SRG output by setting PCR[9:8] for CLKXM = 1 and CLKRM = 1. However, the SRG output is only driven onto the BCLKXn pin because the BCLKR output is automatically disabled.

3.2.3.2 Multichannel Selection

The McBSP supports independent selection of multiple channels for the transmitter and receiver. When multiple channels are selected, each frame represents a time-division multiplexed (TDM) data stream. In using time-division multiplexed data streams, the CPU may only need to process a few of them. Thus, to save memory and bus bandwidth, multichannel selection allows independent enabling of particular channels for transmission and reception. Up to a maximum of 128 channels in a bit stream can be enabled or disabled.

The 5441 McBSPs have two working modes that are selected by setting the RMCME and XMCME bits in the multichannel control registers MCR1x and MCR2x, respectively (see Figure 3−16 and Figure 3−17). For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

- In the first mode, when RMCME = 0 and XMCME = 0, there are two partitions (A and B), with each containing 16 channels as shown in Figure 3−16 and Figure 3−17. This is compatible with the McBSPs used in the 5420, where only 32-channel selection is enabled (default).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						XMCME	XPBBLK		XPABLK		XCBLK			XMCM	
R,+0						RW,+0	RW,+0		RW,+0		R,+0			RW,+0	

LEGEND: R = Read, W = Write, +0 = Value at reset; x = McBSP 0,1, or 2

Figure 3−16. Multichannel Control Register 2 for McBSPx (MCR2x)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						RMCME	RPBBLK		RPABLK		RCBLK			RMCM	
R,+0						RW,+0	RW,+0		RW,+0		R,+0			RW,+0	

LEGEND: R = Read, W = Write, +0 = Value at reset; x = McBSP 0,1, or 2

Figure 3−17. Multichannel Control Register 1 for McBSPx (MCR1x)

- In the second mode, with RMCME = 1 and XMCME = 1, the McBSPs have 128-channel selection capability. Twelve registers (RCERCx−RCERHx and XCERCx−XCERHx) are used to enable the 128-channel selection. The subaddresses of the registers are shown in Table 3−24. These registers, functionally equivalent to the RCERA0−RCERB1 and XCERA0−XCERB1 registers, are used to enable/disable the transmit and receive of additional channel partitions (C,D,E,F,G, and H) in the 128-channel stream. For example, XCERH1 is the transmit enable for channel partition H (channels 112 to 127) of McBSP1 for each DSP subsystem. See Figure 3−18, Table 3−8, Figure 3−19, and Table 3−9 for bit layouts and functions of the receive and transmit registers.

15	14	13	12	11	10	9	8
RCERyz15	RCERyz14	RCERyz13	RCERyz12	RCERyz11	RCERyz10	RCERyz9	RCERyz8
RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0
7	6	5	4	3	2	1	0
RCERyz7	RCERyz6	RCERyz5	RCERy4	RCERyz3	RCERyz2	RCERyz1	RCERyz0
RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0

LEGEND: R = Read, W = Write, +0 = Value at reset; y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2

Figure 3−18. Receive Channel Enable Registers Bit Layout for Partitions A to H

Table 3−8. Receive Channel Enable Registers for Partitions A to H

Bit	Name	Function	
15−0	RCERyz[15:0]	Receive Channel Enable Register	
		RCERyz *n* = 0	Disables reception of *n*th channel in partition y.
		RCERyz *n* = 1	Enables reception of *n*th channel in partition y.

Note: y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2; n = bit 15−0

15	14	13	12	11	10	9	8
XCERyz15	XCERyz14	XCERyz13	XCERyz12	XCERyz11	XCERyz10	XCERyz9	XCERyz8
RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0
7	6	5	4	3	2	1	0
XCERyz7	XCERyz6	XCERyz5	XCERy4	XCERyz3	XCERyz2	XCERyz1	XCERyz0
RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0	RW,+0

LEGEND: R = Read, W = Write, +0 = Value at reset; y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2

Figure 3−19. Transmit Channel Enable Registers Bit Layout for Partitions A to H

Table 3−9. Transmit Channel Enable Registers for Partitions A to H

Bit	Name	Function	
15−0	XCERyz[15:0]	Transmit Channel Enable Register	
		XCERyz *n* = 0	Disables transmit of *n*th channel in partition y.
		XCERyz *n* = 1	Enables transmit of *n*th channel in partition y.

LEGEND: y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2; n = bit 15−0

The McBSP is fully static and operates at arbitrarily low clock frequencies. For the maximum McBSP multichannel operating frequency, see Section 5.9 of this data manual.

3.2.3.3 McBSP1 and McBSP2

The four McBSP1s from each subsystem share the same external signal pins. The four McBSP2s from each subsystem share the same set of external signal pins. They can only operate in either of the following modes:

- multichannel mode (x_BCLKR, x_BCLKX, x_BFSR, and x_BFSX are external and the McBSPs share TDM stream with no single time slot assigned to more than one McBSP)
- standard serial port mode (x_BCLKR, x_BCLKX, x_BFSR, and x_BFSX are external and only one McBSP is enabled at one time).

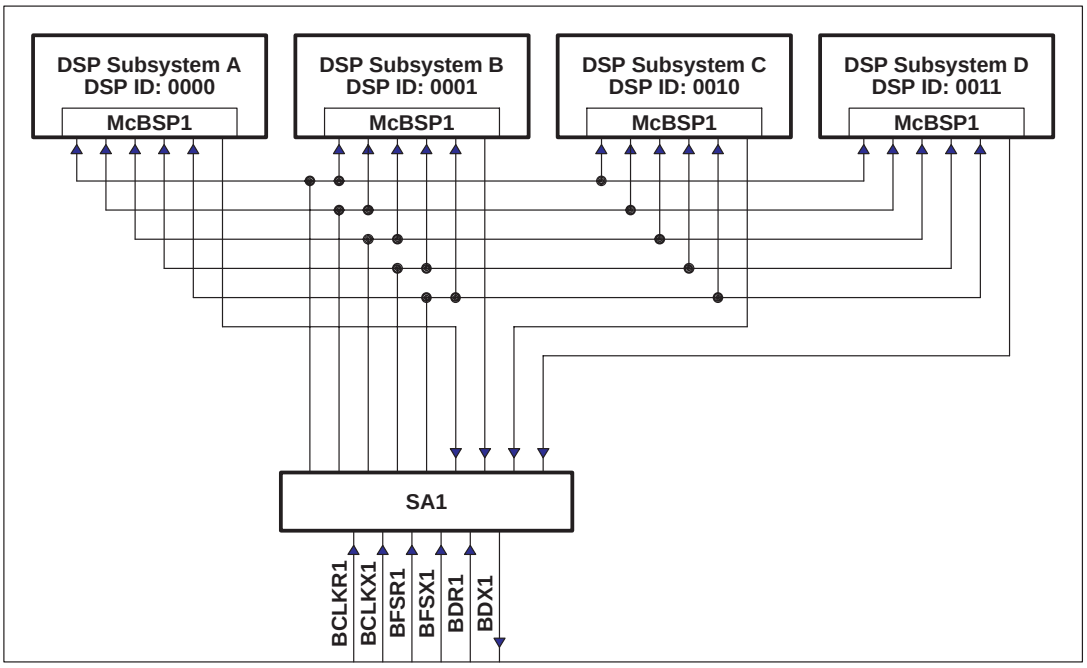
For McBSP1 and McBSP2, no other mode is supported.

3.2.3.4 SA Multiplexer

The SA1 and SA2 multiplexers provide multiplexing for the four McBSP1s and the four McBSP2s from each subsystem and present the data path to the device boundary. All the same functional pins from the four McBSP1s are multiplexed together by SA1 and connect to the device external pins. All the same functional pins from the four McBSP2s are multiplexed together by SA2 and connect to the device external pins. The functional pins are: data receive (BDRn), data transmit (BDXn), receive frame sync (BFSRn), transmit frame sync (BFSXn), receive shift clock (BCLKRn), and transmit shift clock (BCLKXn).

When McBSP operates in multichannel mode, software shall ensure that the same channel (time slot) not be assigned by more than one subsystem. If more than one subsystem enables the same transmit time slot, the results are undefined.

Figure 3−20 shows 5441 block diagram with SA1 logic; SA2 logic is identical.



NOTE: SA is the MUX/Arbitration logic for McBSP1 operation.

Figure 3−20. SA Multiplexer for McBSP1 Operation

3.2.4 Hardware Timer

Each 5441 subsystem has one independent software programmable timer. The memory-mapped registers control the operation of the timer. The timer resolution is the clock rate of the CPU. The timer output shares the pin with GPIO3 and is controlled by GPIO register bit 15.

The timer supports a 32-bit dynamic range. The timer consists of a programmable 16-bit main counter and a programmable prescalar. The main counter is driven by the prescalar, which decrements by one at every CPU clock. Once the prescalar reaches zero, the 16-bit counter decrements by one. When the 16-bit counter decrements to zero, a maskable interrupt (TINT) is generated and the timer output pin (TOUT) asserts an active-high pulse (2H − 2 ns, H = 0.5 clock cycle). The timer output pulse is driven on GPIO3 when the TOUT bit is set to high in the GPIO register. When the timer is configured in continuous mode, the timer counter and prescalar will be reloaded accordingly after the timer counter exhausts. The timer can be stopped, restarted, reset, or disabled via the bits of the timer control register.

There are four 16-bit registers associated with the timer.

- Timer counter register (TIM)
- Timer period register (PRD)
- Timer control register (TCR)
- Timer second control register (TSCR)

3.2.4.1 TIM Register

This register is loaded with the period register (PRD) value and decrements once the PRD value is loaded.

3.2.4.2 PRD Register

This register is used to reload the timer counter register (TIM).

3.2.4.3 TCR Register

This register provides the control and status information. TCR bit fields are shown in Figure 3−21 and described in Table 3−10.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SOFT	FREE	PSC				TRB	TSS	TDDR			
				R/W+0	R/W+0	R/W+0				R/W+0	R/W+0	R/W+0			

LEGEND: R = Read, W = Write, +0 = Value at reset

Figure 3−21. Timer Control Register (TCR)

Table 3−10. TCR Bit Description

BIT NO.	BIT NAME	FUNCTION
15−12	Reserved	Register bit is reserved. Read 0, write has no effect.
11	SOFT	Used in conjunction with the FREE bit to determine the state of the timer when a breakpoint is encountered in the HLL debugger. When FREE = 0 and SOFT = 0 the timer stops immediately. When FREE = 0 and SOFT = 1, the timer stops when the counter decrements to 0.
10	FREE	Used in conjunction with the SOFT bit to determine the state of the timer when a breakpoint is encountered in the HLL debugger. When FREE = 0, the SOFT bit selects the timer mode. When FREE = 1, the timer runs free regardless of the SOFT bit.
9−6	PSC	Timer prescalar counter, used only when PREMD = 0 (in TSCR register) and the prescaler is in direct mode.
5	TRB	Timer reload. When TRB is set, TIM is loaded with the value in the PRD register and the PSC field is loaded with the value in the TDDR field (when prescalar is in direct mode). TRB is always read a 0.
4	TSS	Timer stop status. Stops or starts the timer at reset. TSS is cleared and the timer starts timing. 0 = timer is started 1 = timer is stopped
3−0	TDDR	Timer prescalar. Case 1: When PREMD = 0, TDDR is a 4-bit reload prescalar. When PSC decrements to 0, PSC is loaded with the contents of TDDR. Case 2: When PREMD = 1,TDDR is an indirect prescalar, the contents in TDDR is used to specify the timer prescalar. **TDDR[3:0] — PRESCALAR** 0000 — 0001h 0001 — 0003h 0010 — 0007h 0011 — 000Fh 0100 — 001Fh 0101 — 003Fh 0110 — 007Fh 0111 — 00FFh 1000 — 01FFh 1001 — 03FFh 1010 — 07FFh 1011 — 0FFFh 1100 — 1FFFh 1101 — 3FFFh 1110 — 7FFFh 1111 — FFFFh

3.2.4.4 TSCR Register

This 16-bit register contains bits to set prescalar mode.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved			PREMD	Reserved											
			R/W+0												

LEGEND: R = Read, W = Write, +0 = Value at reset

Figure 3−22. Timer Second Control Register (TSCR)

Table 3−11. TSCR Bit Description

BIT NO.	BIT NAME	FUNCTION
15−13	Reserved	Register bit is reserved. Read 0, write has no effect.
12	PREMD	Prescalar mode select bit. 0 = direct mode, TDDR is a 4-bit reload prescalar (default value after reset). 1 = indirect mode, TDDR is used to select individual prescalar value.
11−0	Reserved	Register bit is reserved. Read 0, write has no effect.

Out of reset, the TIM and PRD registers are set to a maximum value of FFFFh, the PREMD bit (TSCR[12]) is set to 0, the TDDR field (TCR[3:0]) is cleared to 0, and the timer is started.

3.2.5 Watchdog Timer

Each subsystem contains a watchdog timer. The purpose of the watchdog timer is to prevent the system from lock in case the software becomes trapped in loops with no controlled exit. The watchdog timer has a “watchdog output” pin associated with it. This watchdog output pin is shared with the x_GPIO2/$\overline{\text{x\_WTOUT}}$ pin; once the watchdog timer is enabled, this pin is automatically configured as $\overline{\text{x\_WTOUT}}$. The watchdog timer requires a special service sequence to be executed periodically. Without this periodic servicing, the watchdog timer counter reaches zero and times out. Consequently, an active-low pulse will be asserted on the “watchdog output” pin and an internal maskable interrupt will be triggered. The watchdog output ($\overline{\text{x\_WTOUT}}$) pin can be gluelessly external-connected to the local hardware reset or NMI (nonmaskable interrupt). This allows maximum flexibility in utilizing the watchdog as required by the particular application.

The watchdog timer is a prescaled 16-bit counter that supports up to a 32-bit dynamic range. Out of reset, the watchdog is disabled in order to allow as much time as needed for code to be loaded into the 5441 on-chip memory via the HPI. Prior to being enabled, the watchdog counter will, in fact, still count down from its initial default value using the default prescalar value. When the counter reaches zero, a watchdog time-out event will occur in that a WD interrupt (WDTINT) request will be sent to the core, and the WDFLAG will be set. However, since all maskable interrupts are disabled by default at reset, the WDTINT will not be serviced by the core. Additionally, the watchdog pin ($\overline{\text{x\_WTOUT}}$) is disconnected from the watchdog time-out event, so no pulse will be generated on this pin. After this time-out, the counter and prescalar will be reloaded automatically and the watchdog will continue to count, time out, reload, etc. After code-download, the watchdog can be enabled to connect the $\overline{\text{x\_WTOUT}}$ pin to the time-out event. To enable the watchdog, certain sequence shall be followed as shown in Figure 3−25.

Once the watchdog is enabled, it cannot be disabled by software. It can be disabled by watchdog time-out, local hardware reset, or global hardware reset. A special key sequence is provided to prevent the watchdog from being accidentally serviced while the software is trapped in a dead loop or in some other software failures.

3.2.5.1 Watchdog Timer Registers

There are four 16-bit registers associated with the watchdog timer.

- WD Timer Counter Register (WDTIM)
- WD Timer Period Register (WDPRD)
- WD Timer Control Register (WDTCR)
- WD Timer Second Control Register (WDTSCR)

3.2.5.2 WDTIM Register

This register contains the 16-bit watchdog counter value. It is decremented once every watchdog clock cycle.

3.2.5.3 WDPRD Register

This register is used to reload the WD timer counter register (WDTIM).

3.2.5.4 WDTCR Register

This register provides the control and status information. WDTCR bit fields are as shown in Figure 3−23 and are described in Table 3−12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				SOFT	FREE	PSC				Reserved		TDDR			
				R/W+0	R/W+0	R						R/W+1111			

LEGEND: R = Read, W = Write, +0 = Value at reset

Figure 3−23. Watchdog Timer Control Register (WDTCR)

Table 3−12. WDTCR Bit Description

BIT NO.	BIT NAME	FUNCTION
15−12	Reserved	Register bit is reserved. Read 0, write has no effect.
11	SOFT	Used in conjunction with the FREE bit to determine the state of the timer when a breakpoint is encountered in the HLL debugger. When FREE = 0 and SOFT = 0 the timer stops immediately. When FREE = 0 and SOFT = 1, the timer stops when the counter decrements to 0.
10	FREE	Used in conjunction with the SOFT bit to determine the state of the timer when a breakpoint is encountered in the HLL debugger. When FREE = 0, the SOFT bit selects the timer mode. When FREE = 1, the timer runs free regardless of the SOFT bit.
9−6	PSC	Timer prescalar counter, used only when PREMD = 0 (in WDTSCR register) and the prescaler is in direct mode.
5−4	Reserved	Register bit is reserved. Read 0, write has no effect.
3−0	TDDR	Timer prescalar. Case 1: When PREMD = 0, TDDR is a 4-bit reload prescalar. When PSC decrements to 0, PSC is loaded with the contents of TDDR. Case 2: When PREMD = 1,TDDR is an indirect prescalar, the contents in TDDR is used to specify the timer prescalar. **TDDR[3:0] PRESCALAR** 0000 0001h 0001 0003h 0010 0007h 0011 000Fh 0100 001Fh 0101 003Fh 0110 007Fh 0111 00FFh 1000 01FFh 1001 03FFh 1010 07FFh 1011 0FFFh 1100 1FFFh 1101 3FFFh 1110 7FFFh 1111 FFFFh (Default)

3.2.5.5 WDTSCR Register

This 16-bit register contains bits to indicate watchdog flag, to enable watchdog, to set prescalar mode as well as to provide the 12-bit WDKEY for watchdog service.

WDTSCR bit fields are shown in Figure 3−24 and are described in Table 3−13.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDFLAG	WDEN	Reserved	PREMD	WDKEY											
R/W+0	R/W+0		R/W+1	R/W+0											

LEGEND: R = Read, W = Write, +0 = Value at reset

Figure 3−24. Watchdog Timer Second Control Register (WDTSCR)

Table 3−13. WDTSCR Bit Description

BIT NO.	BIT NAME	FUNCTION
15	WDFLAG	Watchdog flag bit. This bit can be cleared by enabling the watchdog timer, by device global reset, and by being written with “1”. It is set by a watchdog time-out. 0 = No watchdog time-out occurred 1 = Watchdog time-out occurred
14	WDEN	Watchdog timer enable bit. 0 = Watchdog disable. Default value after device reset. Watchdog output pin is disconnected to the watchdog time-out event, counter starts to run. 1 = Watchdog enable. Once enabled, the watchdog output pin is connected to the watchdog time-out event, and can be disabled by watchdog time-out or reset.
13	Reserved	Register bit is reserved. Read 0, write has no effect.
12	PREMD	Prescalar mode select bit. 0 = Direct mode, TDDR is 4-bit reload prescalar. 1 = Indirect mode, TDDR is used to select individual prescalar value (default value after local or global hardware reset).
11−0	WDKEY	12-bit watchdog reset key, only the sequence of a 5C6h followed by an A7Eh services the watchdog.

The watchdog has to be serviced periodically with the sequence of 5C6h followed by A7Eh, written to WDKEY before the watchdog timer times out. Both 5C6h and A7Eh are allowed to be written to WDKEY. Only the sequence of 5C6h followed by A7Eh, to WDKEY services the watchdog. Any other writes to WDKEY will trigger the watchdog time-out immediately, and consequently:

- the watchdog output pin will generate an active-low pulse (6H ns, H=0.5 clock cycle)
- the WDFLAG bit in WDTSCR will be set to 1
- the internal maskable WD interrupt (WD_TINT) will be triggered

Read from WDTSCR register will not cause time-out.

When the watchdog is in time-out state, the watchdog is disabled and WDEN is cleared. The watchdog output pin ($\overline{\text{x\_WTOUT}}$) is disconnected to the watchdog time-out event. Finally, the timer is reloaded and continues to run.

Out of reset, the watchdog is disabled, and reads and writes to the watchdog registers are allowed. Once 5C6h is written to WDKEY in the WDTSCR register from the initial state, the watchdog enters the preactive state. The next write to the WDTSCR register should be completed with a “1” written to WDEN and A7Eh written to WDKEY. This causes the watchdog timer to enter the active state. Once the watchdog is enabled, it cannot be disabled by software. Any writes to the WDTSCR register from the active or service states that do not write 5C6h or A7Eh to WDKEY will result in an immediate watchdog time-out. Writing the sequence of 5C6h and A7Eh to WDKEY causes the watchdog timer to transition between the active and service states. The transition from the service state to the active state results in the timer register reload that is necessary to keep the watchdog timer from timing out. Each time the watchdog is serviced by the sequence, the watchdog timer counter and prescalar will automatically be reloaded.

The registers WDTIM, WDPRD, WDTCR, and the PREMD bit in WDTSCR must be configured before the watchdog enters the active state. By default, WDTIM =FFFFh, WDPRD = FFFFh, PREMD = 1, TDDR = 1111b. Writing a ‘1’ to WDEN and configuring the PREMD bit must be done at the same time that A7Eh is written to WDKEY in watchdog pre-active state.

3.2.5.6 Watchdog State Diagram

Figure 3−25 shows the watchdog operation state diagram.

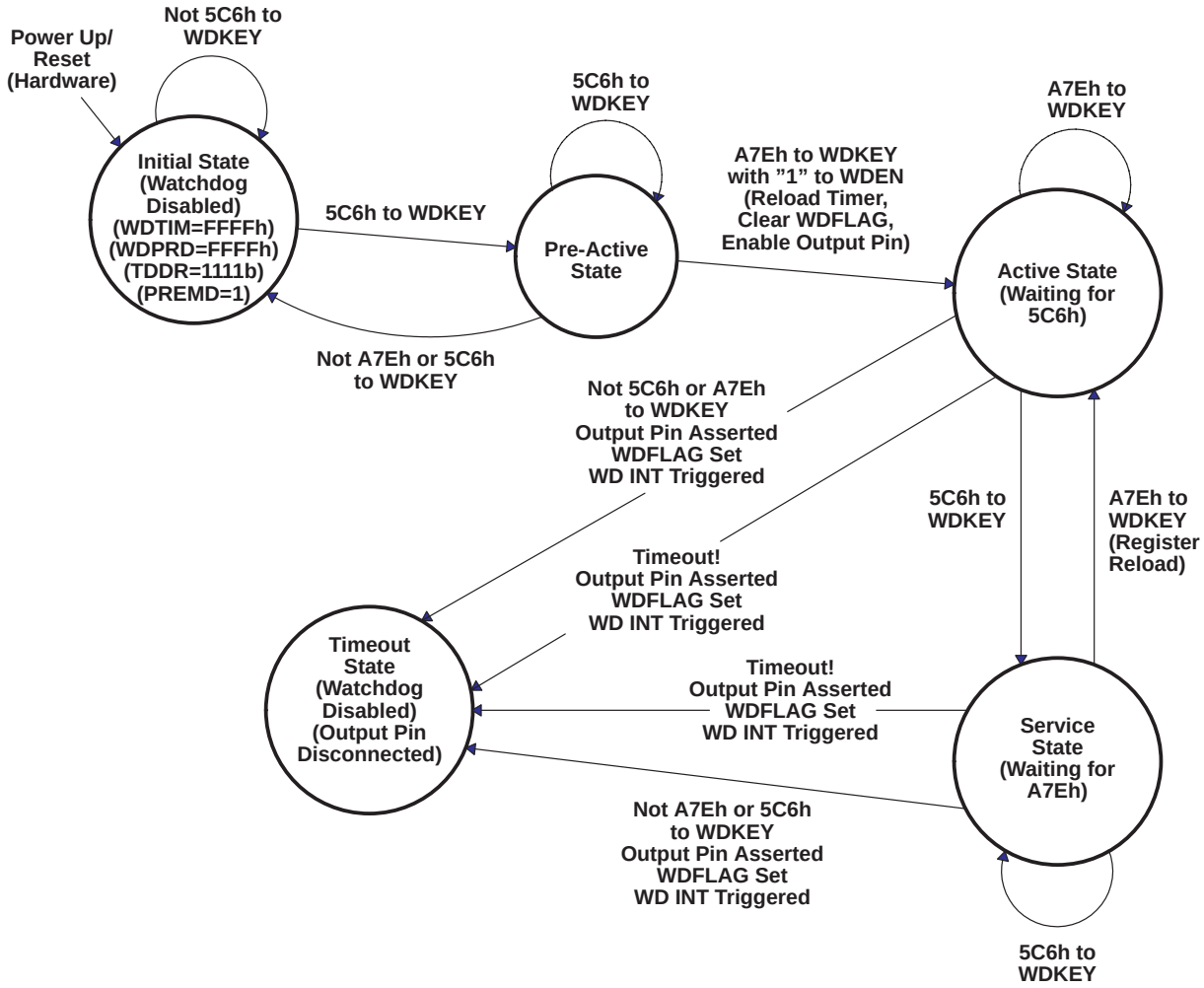


Figure 3−25. Watchdog Operation State Diagram

As shown in Figure 3−25, the watchdog is disabled before it enters the active state. Even though disabled, the WD interrupt (WD_TINT) may be triggered periodically although the watchdog output pin (x_WTOUT) will not be asserted. The interrupt may be utilized to:

- Indicate that watchdog is not in active state
- Allow the watchdog timer to act as a general-purpose time counter if the watchdog functionality is not needed.

3.2.5.7 Watchdog Register Write Protection

Once the watchdog is enabled, writes to registers WDTIM, WDPRD, and WDTCR will have no effect. Writes to the WDFLAG, WDEN, and PREMD bits in register WDTSCR will have no effect. However, writing an incorrect key (not 5C6h or A7Eh) to WDKEY will result in an immediate time-out.

3.2.6 Software-Programmable Phase-Locked Loop (PLL)

The clock generator provides clocks to the 5441 device, and consists of a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which must be provided by using an external clock source. The reference clock input is then divided by two (DIV mode) to generate clocks for the 5441 device. Alternately, the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal. When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock for the 5441 device. Only subsystem A controls the PLL. Subsystems B, C, and D cannot access the PLL registers.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (CLKIN) is multiplied by 1 of 31 possible ratios. These ratios are achieved using the PLL circuitry.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Figure 3−26 shows the bit layout of the clock mode register and Table 3−14 describes the bit functions.

15 12	11	10 3	2	1	0
PLLMUL†	PLLDIV†	PLLCOUNT†	PLLON/OFF†	PLLNDIV	STATUS
R/W	R/W	R/W	R/W	R/W	R/W

† When in DIV mode (PLLSTATUS is low), PLLMUL, PLLDIV, PLLCOUNT, and PLLON/OFF are don't cares, and their contents are indeterminate.

LEGEND: R = Read, W = Write

Figure 3−26. Clock Mode Register (CLKMD)

Table 3−14. Clock Mode Register (CLKMD) Bit Functions

BIT NO.	BIT NAME	FUNCTION
15−12	PLLMUL†	PLL multiplier. PLLMUL defines the frequency multiplier in conjunction with PLLDIV and PLLNDIV. See Table 3−15.
11	PLLDIV†	PLL divider. PLLDIV defines the frequency multiplier in conjunction with PLLMUL and PLLNDIV. See Table 3−15. PLLDIV = 0 Means that an integer multiply factor is used PLLDIV = 1 Means that a noninteger multiply factor is used
10−3	PLLCOUNT†	PLL counter value. PLLCOUNT specifies the number of input clock cycles (in increments of16 cycles) for the PLL lock timer to count before the PLL begins clocking the processor after the PLL is started. The PLL counter is a down-counter, which is driven by the input clock divided by 16; therefore, for every 16 input clocks, the PLL counter decrements by one. The PLL counter can be used to ensure that the processor is not clocked until the PLL is locked, so that only valid clock signals are sent to the device.
2	PLLON/OFF†	PLL on/off. PLLON/OFF enables or disables the PLL part of the clock generator in conjunction with the PLLNDIV bit (see Table 3−16). Note that PLLON/OFF and PLLNDIV can both force the PLL to run; when PLLON/OFF is high, the PLL runs independently of the state of PLLNDIV.
1	PLLNDIV	PLLNDIV configures PLL mode when high or DIV mode when low. PLLNDIV defines the frequency multiplier in conjunction with PLLDIV and PLLMUL. See Table 3−15.
0	STATUS	Indicates the PLL mode. STATUS = 0 Indicates DIV mode STATUS = 1 Indicates PLL mode

† When in DIV mode (PLLSTATUS is low), PLLMUL, PLLDIV, PLLCOUNT, and PLLON/OFF are don't cares, and their contents are indeterminate.

Table 3−15. Multiplier Related to PLLNDIV, PLLDIV, and PLLMUL

PLLNDIV	PLLDIV	PLLMUL	MULTIPLIER‡
0	x	0−14	0.5
0	x	15	0.25
1	0	0−14	PLLMUL + 1
1	0	15	bypass (multiply by 1)
1	1	0 or even	(PLLMUL + 1)/2
1	1	odd	PLLMUL/4

‡ CLKOUT = CLKIN * Multiplier

Table 3−16. VCO Truth Table

PLLON/OFF	PLLNDIV	VCO STATE
0	0	off
1	0	on
0	1	on
1	1	on

3.2.6.1 PLL Clock Programmable Timer

During the lockup period, the PLL should not be used to clock the 5441. The PLLCOUNT programmable lock timer provides a convenient method of automatically delaying clocking of the device by the PLL until lock is achieved.

The PLL lock timer is a counter, loaded from the PLLCOUNT field in the CLKMD register, that decrements from its preset value to 0. The timer can be preset to any value from 0 to 255, and its input clock is CLKIN divided by 16. The resulting lockup delay can therefore be set from 0 to 255 × 16 CLKIN cycles.

The lock timer is activated when the operating mode of the clock generator is switched from DIV to PLL. During the lockup period, the clock generator continues to operate in DIV mode; after the PLL lock timer decrements to zero, the PLL begins clocking the 5441.

Accordingly, the value loaded into PLLCOUNT is chosen based on the following formula:

$$PLLCOUNT = \frac{Lockup\ Time}{16 \times T_{CLKIN}}$$

where T_{CLKIN} is the input reference clock period and lockup time is the required VCO lockup time, as shown in Table 3−17.

Table 3−17. VCO Lockup Time

CLKOUT FREQUENCY (MHz)	LOCKUP TIME (μs)†
5	23
10	17
20	16
40	19
60	24
80	29
100	35
135	45

† Approximate values

3.2.6.2 CLKMD Register Initialization At Reset

The clock mode pin (CLKMD) is used to initialize the PLL to a known value at reset. The CLKMD pin is sampled when the reset signal is low. Only global reset ($\overline{\text{RESET}}$) will reset the PLL. Subsystem A local reset ($\overline{\text{A\_RS}}$) has no effect on the PLL.

Table 3−18. PLL Initialization at Reset

CLKMD PIN	PLL MODE
0	Bypass
1	CLKINx2

3.2.7 General-Purpose I/O

The 5441 has 16 general-purpose I/O pins. These pins are:

A_GPIO0, A_GPIO1, A_GPIO2, A_GPIO3

B_GPIO0, B_GPIO1, B_GPIO2, B_GPIO3

C_GPIO0, C_GPIO1, C_GPIO2, C_GPIO3

D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3

Four bits of general-purpose I/O are available to each core. Each GPIO pin can be individually selected as either an input or an output through the GPIO register. The x_XF, $\overline{\text{x\_BIO}}$, and timer output are selectable on GPIO pins 0, 1, and 3 through the GPIO register also. Each output driver has an independent three-state control. All nonreserved GPIO register bits are readable and writeable. The GPIO register bits will be set to 0 when the core is in reset, which will configure all GPIO as inputs. GPIO data and control bits are accessible through a memory-mapped register at 3Ch with the format shown in Figure 3−27 and the bit functions described in Table 3−19.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOUT	Rsvd	X_BIO	X_XF	GPIO DIR3	GPIO DIR2	GPIO DIR1	GPIO DIR0	CLK OUT1	CLK OUT0	Reserved		GPIO DAT3	GPIO DAT2	GPIO DAT1	GPIO DAT0
R/W+0		R/W+0	R/W+0	R/W+0	R/W+0	R/W+0	R/W+0	R/W+0	R/W+0			R/W+0	R/W+0	R/W+0	R/W+0

LEGEND: R = Read, W = Write, +0 = Value at reset

Figure 3−27. General-Purpose I/O Control Register

Table 3−19. General-Purpose I/O Control Register Bit Functions

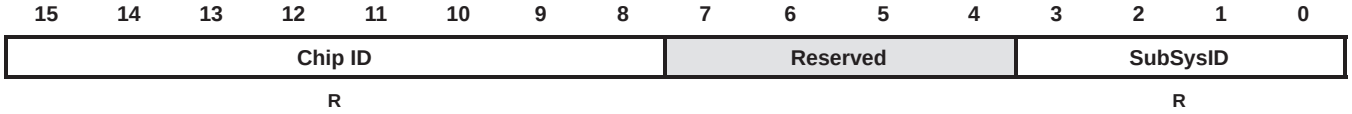
BIT NO.	BIT NAME	BIT VALUE	FUNCTION
15	TOUT	0	Timer output disable. Uses GPIO3 as general-purpose I/O.
		1	Timer output enable. Overrides DIR3. Timer output is driven on GPIO3 and readable in DAT3.
14	Reserved	X	Register bit is reserved. Read 0, write has no effect.
13	X_BIO	0	Branch control input disable. Uses GPIO1 as general-purpose I/O.
		1	Branch control input enable. Overrides DIR1. The X_BIO output is driven on GPIO1 and readable in DAT0.
12	X_XF	0	External flag output disable. Uses GPIO0 as general-purpose I/O.
		1	External flag output enable. Overrides DIR0. The X_XF output is driven on GPIO0 and readable in DAT1.
11−8	GPIO DIRn†	0	GPIOn pin is used as an input.
		1	GPIOn pin is used as an output.
7−6	CLKOUT		CLKOUT muxing selection bits. CLKOUT1[7] CLKOUT0[6] A_CLKOUT (default) 0 0 B_CLKOUT 0 1 C_CLKOUT 1 0 D_CLKOUT 1 1
5−4	Reserved	X	Register bit is reserved. Read 0, write has no effect.
3−0	GPIO DATn†	0	GPIOn is driven with a 0 (DIRn = 1). GPIOn is read as 0 (DIRn = 0).
		1	GPIOn is driven with a 1 (DIRn = 1). GPIOn is read as 1 (DIRn = 0).

† n = 3, 2, 1, or 0

The timer output (TOUT) bit is used to multiplex the output of the timer and GPIO3. The X_XF bit is used to multiplex the output of the external flag, and the X_BIO bit is used to multiplex the input of the branch control. The watchdog enable (WDEN) bit in the watchdog timer second control register (WDTSCR) is used to multiplex the watchdog timer output and GPIO2. All GPIO pins are programmable as an input or output by the direction bit (GPIODIRn). Data is either driven or read from the data bit field (GPIODATn). GPIODIR3 has no effect when TOUT = 1.

3.2.8 Chip Subsystem ID Register

The chip subsystem ID register (CSIDR) is a read-only memory-mapped register located at 3Eh within each DSP subsystem. This register contains two elements for electrically readable device identification. The Chip ID bits identify the type of C54x™ device (41h for 5441). The SubSysID contains a unique subsystem identifier. Figure 3−28 shows the CSIDR and Table 3−20 describes its bit functions.



LEGEND: R = Read

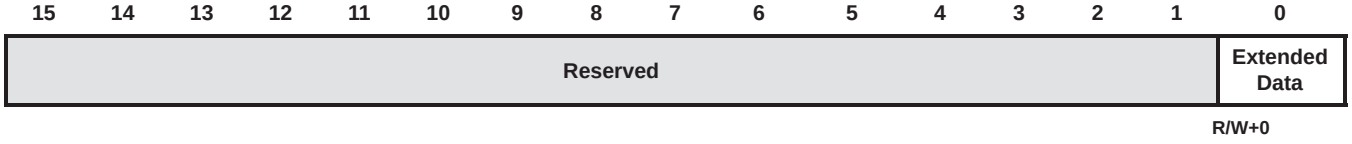
Figure 3−28. Chip Subsystem ID Register (CSIDR)

Table 3−20. Chip Subsystem ID Register Bit Functions

BIT NO.	BIT FIELD NAME	FUNCTION
15−8	Chip ID	54x device type. Contains 41h for 5441.
7−4	Reserved	
3−0	SubSysID	Identifier for DSP subsystem: A = 00b, B = 01b, C = 10b, and D = 11b

3.2.9 Data Memory Map Register

To access the extended data memory, the DSP CPU need to configure the data memory map register (DMMR), which is used to point to extended data memory. The content of DMMR register is used to select the extended data for all CPU data memory accesses. Figure 3−29 shows the DMMR and Table 3−21 describes its bit functions.



LEGEND: R = Read, W = Write

Figure 3−29. Data Memory Map Register (DMMR)

Table 3−21. Data Memory Map Register Functions

BIT NO.	BIT FIELD NAME	FUNCTION
15−1	Reserved	
0	Extended data	Extended data memory for CPU access: Extended_Data = 0b, DARAM2 and DARAM3 are mapped in. Extended_Data = 1b, DARAM4 and DARAM5 are mapped in.

3.3 Memory-Mapped Registers

The 5441 has 27 processor memory-mapped registers, which are mapped in data memory space addresses 0h to 1Fh as shown in Table 3−22. Each device also has a set of memory-mapped registers associated with the peripherals as shown in Table 3−23.

Table 3−22. Processor Memory-Mapped Registers for Each DSP Subsystem

NAME	ADDRESS DEC	ADDRESS HEX	DESCRIPTION
IMR	0	0	Interrupt Mask Register
IFR	1	1	Interrupt Flag Register
—	2−5	2−5	Reserved for testing
ST0	6	6	Status Register 0
ST1	7	7	Status Register 1
AL	8	8	Accumulator A Low Word (15−0)
AH	9	9	Accumulator A High Word (31−16)
AG	10	A	Accumulator A Guard Bits (39−32)
BL	11	B	Accumulator B Low Word (15−0)
BH	12	C	Accumulator B High Word (31−16)
BG	13	D	Accumulator B Guard Bits (39−32)
TREG	14	E	Temporary Register
TRN	15	F	Transition Register
AR0	16	10	Auxiliary Register 0
AR1	17	11	Auxiliary Register 1
AR2	18	12	Auxiliary Register 2
AR3	19	13	Auxiliary Register 3
AR4	20	14	Auxiliary Register 4
AR5	21	15	Auxiliary Register 5
AR6	22	16	Auxiliary Register 6
AR7	23	17	Auxiliary Register 7
SP	24	18	Stack Pointer
BK	25	19	Circular Buffer Size Register
BRC	26	1A	Block-Repeat Counter
RSA	27	1B	Block-Repeat Start Address
REA	28	1C	Block-Repeat End Address
PMST	29	1D	Processor Mode Status Register
XPC	30	1E	Extended Program Counter
—	31	1F	Reserved

Table 3−23. Peripheral Memory-Mapped Registers for Each DSP Subsystem

NAME	ADDRESS (HEX)	DESCRIPTION
DRR20	20	McBSP 0 Data Receive Register 2
DRR10	21	McBSP 0 Data Receive Register 1
DXR20	22	McBSP 0 Data Transmit Register 2
DXR10	23	McBSP 0 Data Transmit Register 1
TIM	24	Timer Register
PRD	25	Timer Period Register
TCR	26	Timer Control Register
TSCR	27	Timer Second Control Register
−	28	Reserved
BSCR	29	Bank-Switching Control Register
—	2A−2B	Reserved
HPIC	2C	HPI Control Register (HMODE=0 only)
—	2D−2F	Reserved
DRR22	30	McBSP 2 Data Receive Register 2
DRR12	31	McBSP 2 Data Receive Register 1
DXR22	32	McBSP 2 Data Transmit Register 2
DXR12	33	McBSP 2 Data Transmit Register 1
SPSA2	34	McBSP 2 Subbank Address Register†
SPSD2	35	McBSP 2 Subbank Data Register†
—	36−37	Reserved
SPSA0	38	McBSP 0 Subbank Address Register†
SPSD0	39	McBSP 0 Subbank Data Register†
—	3A−3B	Reserved
GPIO	3C	General-Purpose I/O Register
—	3D	Reserved
CSIDR	3E	Chip Subsystem ID register
—	3F	Reserved
DRR21	40	McBSP 1 Data Receive Register 2
DRR11	41	McBSP 1 Data Receive Register 1
DXR21	42	McBSP 1 Data Transmit Register 2
DXR11	43	McBSP 1 Data Transmit Register 1
—	44−47	Reserved
SPSA1	48	McBSP 1 Subbank Address Register†
SPSD1	49	McBSP 1 Subbank Data Register†
—	4A−4B	Reserved
TIM	4C	Watchdog Timer Register
PRD	4D	Watchdog Timer Period Register
TCR	4E	Watchdog Timer Control Register
WDTSCR	4F	Watchdog Timer Second Control Register
DMMR	50	Data Memory Map Register
—	51−53	Reserved
DMPREC	54	DMA Priority and Enable Control Register
DMSA	55	DMA Subbank Address Register‡
DMSDI	56	DMA Subbank Data Register with Autoincrement‡

†See Table 3−24 for a detailed description of the McBSP control registers and their subaddresses.
‡See Table 3−25 for a detailed description of the DMA subbank addressed registers.

Table 3−23. Peripheral Memory-Mapped Registers for Each DSP Subsystem (Continued)

NAME	ADDRESS (HEX)	DESCRIPTION
DMSDN	57	DMA Subbank Data Register‡
CLKMD	58	Clock Mode Register (CLKMD), subsystem A only (reserved in subsystems B, C, and D)
—	59−5F	Reserved

†See Table 3−24 for a detailed description of the McBSP control registers and their subaddresses.
‡See Table 3−25 for a detailed description of the DMA subbank addressed registers.

3.4 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The McBSP subbank address register (SPSAx) is used as a pointer to select a particular register within the subbank. The McBSP data register (SPSDx) is used to access (read or write) the selected register. Table 3−24 shows the McBSP control registers and their corresponding subaddresses.

Table 3−24. McBSP Control Registers and Subaddresses

McBSP0		McBSP1		McBSP2		SUB-ADDRESS	DESCRIPTION
NAME	ADDRESS	NAME	ADDRESS	NAME	ADDRESS		
SPCR10	39h	SPCR11	49h	SPCR12	35h	00h	Serial port control register 1
SPCR20	39h	SPCR21	49h	SPCR22	35h	01h	Serial port control register 2
RCR10	39h	RCR11	49h	RCR12	35h	02h	Receive control register 1
RCR20	39h	RCR21	49h	RCR22	35h	03h	Receive control register 2
XCR10	39h	XCR11	49h	XCR12	35h	04h	Transmit control register 1
XCR20	39h	XCR21	49h	XCR22	35h	05h	Transmit control register 2
SRGR10	39h	SRGR11	49h	SRGR12	35h	06h	Sample rate generator register 1
SRGR20	39h	SRGR21	49h	SRGR22	35h	07h	Sample rate generator register 2
MCR10	39h	MCR11	49h	MCR12	35h	08h	Multichannel register 1
MCR20	39h	MCR21	49h	MCR22	35h	09h	Multichannel register 2
RCERA0	39h	RCERA1	49h	RCERA2	35h	0Ah	Receive channel enable register partition A
RCERB0	39h	RCERB1	49h	RCERB2	35h	0Bh	Receive channel enable register partition B
XCERA0	39h	XCERA1	49h	XCERA2	35h	0Ch	Transmit channel enable register partition A
XCERB0	39h	XCERB1	49h	XCERB2	35h	0Dh	Transmit channel enable register partition B
PCR0	39h	PCR1	49h	PCR2	35h	0Eh	Pin control register
RCERC0	39h	RCERC1	49h	RCERC2	35h	010h	Receive channel enable register partition C
RCERD0	39h	RCERD1	49h	RCERD2	35h	011h	Receive channel enable register partition D
XCERC0	39h	XCERC1	49h	XCERC2	35h	012h	Transmit channel enable register partition C
XCERD0	39h	XCERD1	49h	XCERD2	35h	013h	Transmit channel enable register partition D
RCERE0	39h	RCERE1	49h	RCERE2	35h	014h	Receive channel enable register partition E
RCERF0	39h	RCERF1	49h	RCERF2	35h	015h	Receive channel enable register partition F
XCERE0	39h	XCERE1	49h	XCERE2	35h	016h	Transmit channel enable register partition E
XCERF0	39h	XCERF1	49h	XCERF2	35h	017h	Transmit channel enable register partition F
RCERG0	39h	RCERG1	49h	RCERG2	35h	018h	Receive channel enable register partition G
RCERH0	39h	RCERH1	49h	RCERH2	35h	019h	Receive channel enable register partition H
XCERG0	39h	XCERG1	49h	XCERG2	35h	01Ah	Transmit channel enable register partition G
XCERH0	39h	XCERH1	49h	XCERH2	35h	01Bh	Transmit channel enable register partition H

3.5 DMA Subbank Addressed Registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSDN) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically postincremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank. Table 3−25 shows the DMA controller subbank addressed registers and their corresponding subaddresses.

Table 3−25. DMA Subbank Addressed Registers

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMSRC0	56h/57h	00h	DMA channel 0 source address register
DMDST0	56h/57h	01h	DMA channel 0 destination address register
DMCTR0	56h/57h	02h	DMA channel 0 element count register
DMSFC0	56h/57h	03h	DMA channel 0 sync select and frame count register
DMMCR0	56h/57h	04h	DMA channel 0 transfer mode control register
DMSRC1	56h/57h	05h	DMA channel 1 source address register
DMDST1	56h/57h	06h	DMA channel 1 destination address register
DMCTR1	56h/57h	07h	DMA channel 1 element count register
DMSFC1	56h/57h	08h	DMA channel 1 sync select and frame count register
DMMCR1	56h/57h	09h	DMA channel 1 transfer mode control register
DMSRC2	56h/57h	0Ah	DMA channel 2 source address register
DMDST2	56h/57h	0Bh	DMA channel 2 destination address register
DMCTR2	56h/57h	0Ch	DMA channel 2 element count register
DMSFC2	56h/57h	0Dh	DMA channel 2 sync select and frame count register
DMMCR2	56h/57h	0Eh	DMA channel 2 transfer mode control register
DMSRC3	56h/57h	0Fh	DMA channel 3 source address register
DMDST3	56h/57h	10h	DMA channel 3 destination address register
DMCTR3	56h/57h	11h	DMA channel 3 element count register
DMSFC3	56h/57h	12h	DMA channel 3 sync select and frame count register
DMMCR3	56h/57h	13h	DMA channel 3 transfer mode control register
DMSRC4	56h/57h	14h	DMA channel 4 source address register
DMDST4	56h/57h	15h	DMA channel 4 destination address register
DMCTR4	56h/57h	16h	DMA channel 4 element count register
DMSFC4	56h/57h	17h	DMA channel 4 sync select and frame count register
DMMCR4	56h/57h	18h	DMA channel 4 transfer mode control register
DMSRC5	56h/57h	19h	DMA channel 5 source address register
DMDST5	56h/57h	1Ah	DMA channel 5 destination address register
DMCTR5	56h/57h	1Bh	DMA channel 5 element count register
DMSFC5	56h/57h	1Ch	DMA channel 5 sync select and frame count register
DMMCR5	56h/57h	1Dh	DMA channel 5 transfer mode control register
DMSRCP	56h/57h	1Eh	DMA source program page address (common channel)

Table 3−25. DMA Subbank Addressed Registers (Continued)

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMDSTP	56h/57h	1Fh	DMA destination program page address (common channel)
DMIDX0	56h/57h	20h	DMA element index address register 0
DMIDX1	56h/57h	21h	DMA element index address register 1
DMFRI0	56h/57h	22h	DMA frame index register 0
DMFRI1	56h/57h	23h	DMA frame index register 1
DMGSA0	56h/57h	24h	DMA channel 0 global source address reload register
DMGDA0	56h/57h	25h	DMA channel 0 global destination address reload register
DMGCR0	56h/57h	26h	DMA channel 0 global count reload register
DMGFR0	56h/57h	27h	DMA channel 0 global frame count reload register
−	56h/57h	28h	Reserved
−	56h/57h	29h	Reserved
DMGSA1	56h/57h	2Ah	DMA channel 1 global source address reload register
DMGDA1	56h/57h	2Bh	DMA channel 1 global destination address reload register
DMGCR1	56h/57h	2Ch	DMA channel 1 global count reload register
DMGFR1	56h/57h	2Dh	DMA channel 1 global frame count reload register
DMGSA2	56h/57h	2Eh	DMA channel 2 global source address reload register
DMGDA2	56h/57h	2Fh	DMA channel 2 global destination address reload register
DMGCR2	56h/57h	30h	DMA channel 2 global count reload register
DMGFR2	56h/57h	31h	DMA channel 2 global frame count reload register
DMGSA3	56h/57h	32h	DMA channel 3 global source address reload register
DMGDA3	56h/57h	33h	DMA channel 3 global destination address reload register
DMGCR3	56h/57h	34h	DMA channel 3 global count reload register
DMGFR3	56h/57h	35h	DMA channel 3 global frame count reload register
DMGSA4	56h/57h	36h	DMA channel 4 global source address reload register
DMGDA4	56h/57h	37h	DMA channel 4 global destination address reload register
DMGCR4	56h/57h	38h	DMA channel 4 global count reload register
DMGFR4	56h/57h	39h	DMA channel 4 global frame count reload register
DMGSA5	56h/57h	3Ah	DMA channel 5 global source address reload register
DMGDA5	56h/57h	3Bh	DMA channel 5 global destination address reload register
DMGCR5	56h/57h	3Ch	DMA channel 5 global count reload register
DMGFR5	56h/57h	3Dh	DMA channel 5 global frame count reload register
DMSRCDP0	56h/57h	3Eh	DMA channel 0 extended source data page register
DMDSTDP0	56h/57h	3Fh	DMA channel 0 extended destination data page register
DMSRCDP1	56h/57h	40h	DMA channel 1 extended source data page register
DMDSTDP1	56h/57h	41h	DMA channel 1 extended destination data page register
DMSRCDP2	56h/57h	42h	DMA channel 2 extended source data page register
DMDSTDP2	56h/57h	43h	DMA channel 2 extended destination data page register
DMSRCDP3	56h/57h	44h	DMA channel 3 extended source data page register
DMDSTDP3	56h/57h	45h	DMA channel 3 extended destination data page register
DMSRCDP4	56h/57h	46h	DMA channel 4 extended source data page register
DMDSTDP4	56h/57h	47h	DMA channel 4 extended destination data page register

Table 3−25. DMA Subbank Addressed Registers (Continued)

NAME	ADDRESS	SUB-ADDRESS	DESCRIPTION
DMSRCDP5	56h/57h	48h	DMA channel 5 extended source data page register
DMDSTDP5	56h/57h	49h	DMA channel 5 extended destination data page register

3.6 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 3−26.

Table 3−26. 5441 Interrupt Locations and Priorities for Each DSP Subsystem

NAME	LOCATION		PRIORITY	FUNCTION
	DECIMAL	HEX		
$\overline{\text{RS}}$, SINTR	0	00	1	Reset (Hardware and Software Reset)
$\overline{\text{NMI}}$, SINT16	4	04	2	Nonmaskable Interrupt
SINT17	8	08	—	Software Interrupt #17
SINT18	12	0C	—	Software Interrupt #18
SINT19	16	10	—	Software Interrupt #19
SINT20	20	14	—	Software Interrupt #20
SINT21	24	18	—	Software Interrupt #21
SINT22	28	1C	—	Software Interrupt #22
SINT23	32	20	—	Software Interrupt #23
SINT24	36	24	—	Software Interrupt #24
SINT25	40	28	—	Software Interrupt #25
SINT26	44	2C	—	Software Interrupt #26
SINT27	48	30	—	Software Interrupt #27
SINT28	52	34	—	Software Interrupt #28
SINT29	56	38	—	Software Interrupt #29
SINT30	60	3C	—	Software Interrupt #30
$\overline{\text{INT}}$, SINT0	64	40	3	External User Interrupt
WDTINT, SINT1	68	44	4	Watchdog Timer Interrupt
$\overline{\text{INT2}}$, SINT2	72	48	5	Software interrupt #2
TINT, SINT3	76	4C	6	External Timer Interrupt
BRINT0, SINT4	80	50	7	BSP #0 Receive Interrupt
BXINT0, SINT5	84	54	8	BSP #0 Transmit Interrupt
BRINT2, DMAC0	88	58	9	BSP #2 Receive Interrupt or DMA Channel 0
BXINT2, DMAC1	92	5C	10	BSP #2 Receive Interrupt or DMA Channel 1
$\overline{\text{INT3}}$, SINT8	96	60	11	Software interrupt #8
HPINT, SINT9	100	64	12	HPI Interrupt (from DSPINT in HPIC)
BRINT1, DMAC2	104	68	13	BSP #1 Receive Interrupt or DMA Channel 2
BXINT1, DMAC3	108	6C	14	BSP #1 transmit Interrupt or DMA channel 3
DMAC4, SINT12	112	70	15	DMA Channel 4
DMAC5, SINT13	116	74	16	DMA Channel 5
—	120−127	78−7F	—	Reserved

Figure 3−30 shows the bit layout of the IMR and the IFR. Table 3−27 describes the bit functions.

15	14	13	12	11	10	9	8
Reserved		DMAC5	DMAC4	XINT1 or DMAC3	RINT1 or DMAC2	HPINT	Reserved
		R/W	R/W	R/W	R/W	R/W	

7	6	5	4	3	2	1	0
XINT2 or DMAC1	RINT2 or DMAC0	XINT0	RINT0	TINT	Reserved	WDTINT	INT
R/W	R/W	R/W	R/W	R/W		R/W	R/W

LEGEND: R = Read, W = Write

Figure 3−30. Bit Layout of the IMR and IFR Registers for Each Subsystem

Table 3−27. Bit Functions for IMR and IFR Registers for Each DSP Subsystem

BIT NO.	BIT NAME	BIT VALUE	FUNCTION
15−14	Reserved	X	Register bit is reserved.
13	DMAC5	0	IFR/IMR: DMA Channel 5 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: DMA Channel 5 has an interrupt pending/is enabled.
12	DMAC4	0	IFR/IMR: DMA Channel 4 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: DMA Channel 4 has an interrupt pending/is enabled.
11	XINT1	0	IFR/IMR: McBSP_1 has no transmit interrupt pending/is disabled (masked).
		1	IFR/IMR: McBSP_1 has a transmit interrupt pending/is enabled.
	DMAC3	0	IFR/IMR: DMA Channel 3 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: DMA Channel 3 has an interrupt pending/is enabled.
10	RINT1	0	IFR/IMR: McBSP_1 has no receive interrupt pending/is disabled (masked).
		1	IFR/IMR: McBSP_1 has a receive interrupt pending/is enabled.
	DMAC2	0	IFR/IMR: DMA Channel 2 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: DMA Channel 2 has an interrupt pending/is enabled.
9	HPINT	0	IFR/IMR: Host-port interface has no DSPINT interrupt pending/is disabled (masked).
		1	IFR/IMR: Host-port interface has an DSPINT interrupt pending/is enabled.
8	Reserved	X	Register bit is reserved.
7	XINT2	0	IFR/IMR: McBSP_2 has no transmit interrupt pending/is disabled (masked).
		1	IFR/IMR: McBSP_2 has a transmit interrupt pending/is enabled.
	DMAC1	0	IFR/IMR: DMA Channel 1 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: DMA Channel 1 has an interrupt pending/is enabled.
6	RINT2	0	IFR/IMR: McBSP_2 has no receive interrupt pending/is disabled (masked).
		1	IFR/IMR: McBSP_2 has a receive interrupt pending/is enabled.
	DMAC0	0	IFR/IMR: DMA Channel 0 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: DMA Channel 0 has an interrupt pending/is enabled.
5	XINT0	0	IFR/IMR: McBSP_0 has no receive interrupt pending/is disabled (masked).
		1	IFR/IMR: McBSP_0 has a receive interrupt pending/is enabled.
4	RINT0	0	IFR/IMR: McBSP_0 has no receive interrupt pending/is disabled (masked).
		1	IFR/IMR: McBSP_0 has a receive interrupt pending/is enabled.

Table 3−27. Bit Functions for IMR and IFR Registers for Each DSP Subsystem (Continued)

BIT NO.	BIT NAME	BIT VALUE	FUNCTION
3	TINT	0	IFR/IMR: Timer has no interrupt pending/is disabled (masked).
		1	IFR/IMR: Timer has an interrupt pending/is enabled.
2	Reserved	X	Register bit is reserved.
1	WDTINT	0	IFR/IMR: Watchdog interrupt has no interrupt pending/is disabled (masked).
		1	IFR/IMR: Watchdog interrupt has an interrupt pending/is enabled.
0	INT	0	IFR/IMR: Ext user interrupt pin 0 has no interrupt pending/is disabled (masked).
		1	IFR/IMR: Ext user interrupt pin 0 has an interrupt pending/is enabled.

3.7 IDLE3 Power-Down Mode

The IDLE1 and IDLE2 power-down modes operate as described in the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). The IDLE3 mode is special in that the clocking circuitry is shut off to conserve power. The 5441 cannot enter an IDLE3 mode unless all the subsystems execute an IDLE3 instruction. The power-reduced benefits of IDLE3 cannot be realized until all the subsystems enter the IDLE3 state and the internal clocks are automatically shut off. The order in which subsystems enter IDLE3 does not matter.

3.8 Emulating the 5441 Device

The 5441 is a single device, but actually consists of four independent subboundary systems that contain register/status information used by the emulator tools. Code Composer Studio™ has a setup wizard called “Code Composer Setup.” The setup wizard prompts the user for the I/O address of the XDSSIO card and the number of processors in the system. The **board.dat** file is then created and placed in the correct directory automatically. The **board.dat** file contents would look something like this:

“CPU_D” TI320C5xx

“CPU_C” TI320C5xx

“CPU_B” TI320C5xx

“CPU_A” TI320C5xx

The subsystems are serially connected together internally. Emulation information is serially transmitted into the device using TDI. The device responds with serial scan information transmitted out the TDO pin.

Code Composer Studio is a trademark of Texas Instruments.

4 Documentation Support

Extensive documentation supports all TMS320™ DSP family of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the C5000™ platform of DSPs:

- *TMS320C54x™ DSP Functional Overview* (literature number SPRU307)
- Device-specific data sheets
- Complete User Guides
- Development-support tools
- Hardware and software application reports

The five-volume *TMS320C54x DSP Reference Set* (literature number SPRU210) consists of:

- *Volume 1: CPU and Peripherals* (literature number SPRU131)
- *Volume 2: Mnemonic Instruction Set* (literature number SPRU172)
- *Volume 3: Algebraic Instruction Set* (literature number SPRU179)
- *Volume 4: Applications Guide* (literature number SPRU173)
- *Volume 5: Enhanced Peripherals* (literature number SPRU302)

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Information regarding Texas Instruments (TI) DSP products is also available on the Worldwide Web at *http://www.ti.com* uniform resource locator (URL).

TMS320 and C5000 are trademarks of Texas Instruments.

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320VC5441 DSP.

Leading “x” in signal names identifies the subsystem; x = A, B, C, or D for subsystem A, B, C, or D, respectively. Trailing “n” in signal names identifies the McBSP; n = 0, 1, or 2 for McBSP0, McBSP1, or McBSP2, respectively.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 5.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V_{SS}. Figure 5−1 provides the test load circuit values for a 3.3-V device.

Supply voltage I/O range, DV_{DD} . . . . . − 0.3 V to 4.0 V
Supply voltage core range, CV_{DD} . . . . . − 0.3 V to 2.0 V
Supply voltage analog PLL, V_{CCA} . . . . . − 0.3 V to 2.0 V
Input voltage range, V_I . . . . . − 0.5 V to DV_{DD} + 0.5 V
Output voltage range, V_o . . . . . − 0.5 V to DV_{DD} + 0.5 V
Operating case temperature range, T_C (Commercial) . . . . . 0°C to 85°C
T_C (Industrial) . . . . . −40°C to 100°C
Storage temperature range T_{stg} . . . . . − 65°C to 150°C

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
DV_{DD}	Device supply voltage, I/O†		3	3.3	3.6	V
CV_{DD}	Device supply voltage, core†		1.55	1.6	1.65	V
V_{CCA}	Device supply voltage, PLL		1.55	1.6	1.65	V
V_{SS}	Supply voltage, GND			0		V
V_{IH}	High-level input voltage, I/O	Schmitt triggered inputs DV_{DD} = 3.3 ± 0.3 V	0.7DV_{DD}		DV_{DD} + 0.3	V
		All other inputs	2		DV_{DD} + 0.3	
V_{IL}	Low-level input voltage, I/O	Schmitt triggered inputs DV_{DD} = 3.3 ± 0.3 V	0		0.3DV_{DD}	V
		All other inputs	0		0.8	
I_{OH}	High-level output current				− 1	mA
I_{OL}	Low-level output current				1.5	mA
T_C	Operating case temperature, Commercial		0		85	°C
	Operating case temperature, Industrial		−40		100	

† Texas Instrument DSPs do not require specific power sequencing between the core supply and the I/O supply. However, systems should be designed to ensure that neither supply is powered up for extended periods of time if the other supply is below the proper operating voltage. Excessive exposure to these conditions can adversely affect the long-term reliability of the devices. System-level concerns such as bus contention may require supply sequencing to be implemented. In this case, the core supply should be powered up at the same time as or prior to the I/O buffers, and then powered down after the I/O buffers.

5.3 Electrical Characteristics Over Recommended Operating Case Temperature Range (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage‡		V_{DD} = 3.3 ± 0.3 V, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage‡		I_{OL} = MAX			0.4	V
I_{IZ}	Input current in high impedance		V_{DD} = MAX, V_O = V_{SS} to V_{DD}	−10		10	µA
I_I	Input current (V_I = V_{SS} to V_{DD})	$\overline{TRST}$	With internal pulldown	10		300	µA
		See pin descriptions	With internal pullups	−300		−10	
		D[15:0], HA[18:0]	Bus holders enabled, V_{DD} = MAX‖	−275		275	
		All other input-only pins		−10		10	
I_{DDC}	Supply current, all four core CPUs		CV_{DD} = 1.6 V, f_x = 133 MHz§, T_C = 25°C		200¶		mA
I_{DDP}	Supply current, pins		DV_{DD} = 3.3 V, f_{clock} = 133 MHz¶, T_C = 25°C#		40		mA
I_{DDA}	Supply current, PLL				3		mA
I_{DDC}	Supply current, standby	IDLE2	PLL × n mode, 20 MHz input		10		mA
		IDLE3	PLL x n mode, 20 MHz input		3		mA
C_i	Input capacitance				5		pF
C_o	Output capacitance				5		pF

† All values are typical unless otherwise specified.

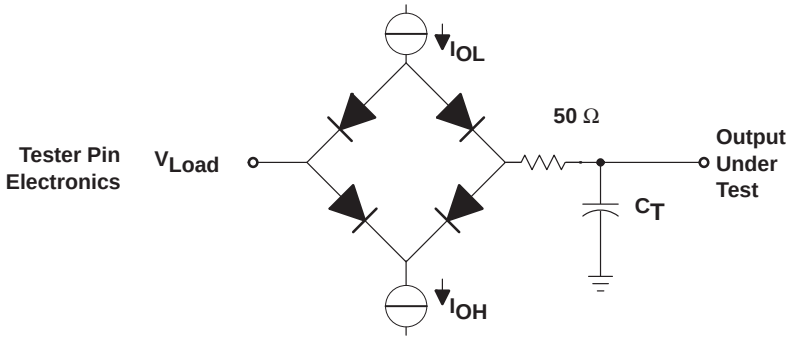
‡ All input and output voltage levels except x_RS, x_INT, x_NMI, CLKIN, x_BCLKX0, x_BCLKR0, BCLKX2, BCLKR2, HAS, HCS, HDS1, HDS2, and RESET are LVTTL-compatible.

§ Clock mode: PLL × 1 with external source

¶ This value is based on 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with the program being executed.

This value was obtained using the following conditions: HPI in multiplexed mode with address autoincrement, HPI read, CLKOFF = 0, full-duplex operation of all 12 McBSPs at a rate of 10 million bits per second each, and 15-pF loads on all outputs. For more details on how this calculation is performed, refer to the *Calculation of TMS320LC54x Power Dissipation Application Report* (literature number SPRA164).

‖ $V_{IL(MIN)} \le V_I \le V_{IL(MAX)}$ or $V_{IH(MIN)} \le V_I \le V_{IH(MAX)}$



Where: I_{OL} = 1.5 mA (all outputs)
I_{OH} = 300 µA (all outputs)
V_{Load} = 1.6 V
C_T = 20 pF typical load circuit capacitance

Figure 5−1. 3.3-V Test Load Circuit

5.4 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

a	access time
c	cycle time (period)
d	delay time
dis	disable time
en	enable time
f	fall time
h	hold time
r	rise time
su	setup time
t	transition time
v	valid time
w	pulse duration (width)
X	Unknown, changing, or don't care level

Letters and symbols and their meanings:

H	High
L	Low
V	Valid
Z	High impedance

5.5 Clock Options

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in Section 3.2.6.

5.5.1 Divide-By-Two, Divide-By-Four, and Bypass Clock Options − PLL Disabled

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in Section 3.2.6.

Table 5−1 and Table 5−2 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−2).

Table 5−1. Divide-By-Two, Divide-By-Four, and Bypass Clock Options Timing Requirements

		MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, CLKIN	20	†	ns
$t_{f(CI)}$	Fall time, CLKIN		6	ns
$t_{r(CI)}$	Rise time, CLKIN		6	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low	5		ns
$t_{w(CIH)}$	Pulse duration, CLKIN high	5		ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.

Table 5−2. Divide-By-Two, Divide-By-Four, and Bypass Clock Options Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	7.5	$2t_{c(CI)}$	†	ns
$t_{c(CO)}$	Cycle time, CLKOUT − bypass mode	7.5	$2t_{c(CI)}$	†	ns
$t_{d(CIH-CO)}$	Delay time, CLKIN high to CLKOUT high/low	2	7	11	ns
$t_{f(CO)}$	Fall time, CLKOUT		1		ns
$t_{r(CO)}$	Rise time, CLKOUT		1		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H−2	H−1	H	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H−2	H−1	H	ns

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞. The device is characterized at frequencies approaching 0 Hz.

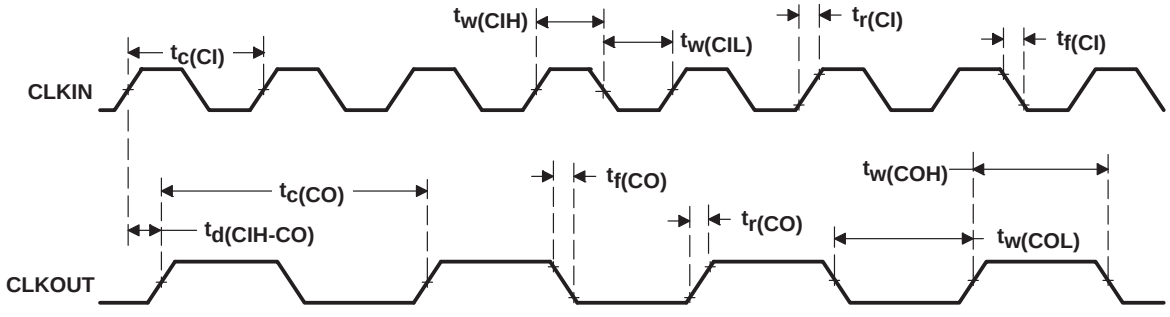


Figure 5−2. External Divide-by-Two Clock Timing

5.5.2 Multiply-By-N Clock Option − PLL Enabled

The frequency of the reference clock provided at the CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in Section 3.2.6.

Table 5−3 and Table 5−4 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−3).

Table 5−3. Multiply-By-N Clock Option Timing Requirements

			MIN	MAX	UNIT
$t_{c(CI)}$	Cycle time, CLKIN	Integer PLL multiplier N (N = 1−15)†	20‡	200	ns
		PLL multiplier N = x.5†	20‡	100	
		PLL multiplier N = x.25, x.75†	20‡	50	
$t_{f(CI)}$	Fall time, CLKIN			6	ns
$t_{r(CI)}$	Rise time, CLKIN			6	ns
$t_{w(CIL)}$	Pulse duration, CLKIN low		5		ns
$t_{w(CIH)}$	Pulse duration, CLKIN high		5		ns

† N = Multiplication factor

‡ The multiplication factor and minimum CLKIN cycle time should be chosen such that the resulting CLKOUT cycle time is within the specified range ($t_{c(CO)}$)

Table 5−4. Multiply-By-N Clock Option Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(CO)}$	Cycle time, CLKOUT	7.5	$t_{c(CI)}/N$†		ns
$t_{d(CI-CO)}$	Delay time, CLKIN high/low to CLKOUT high/low	2	7	11	ns
$t_{f(CO)}$	Fall time, CLKOUT		1.5		ns
$t_{r(CO)}$	Rise time, CLKOUT		1.5		ns
$t_{w(COL)}$	Pulse duration, CLKOUT low	H−2	H−1	H	ns
$t_{w(COH)}$	Pulse duration, CLKOUT high	H−2	H−1	H	ns
t_p	Transitory phase, PLL lock up time			45	μs

† N = Multiplication factor

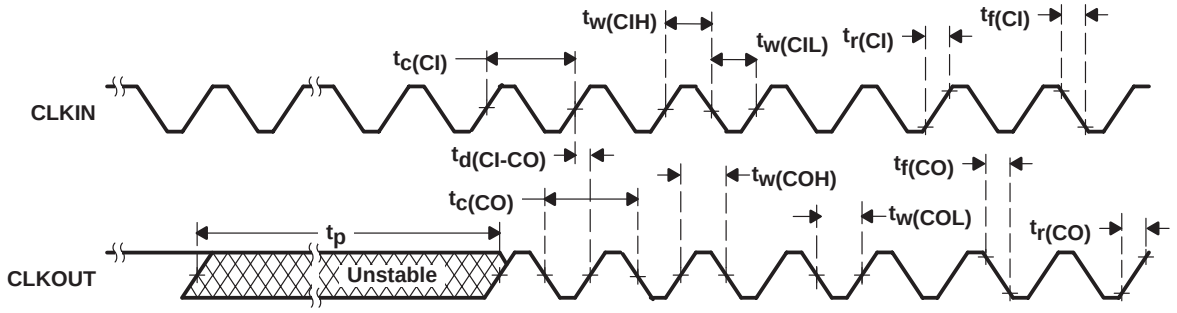


Figure 5−3. External Multiply-by-One Clock Timing

5.6 Reset, x_BIO, and Interrupt Timings

Table 5−5 assumes testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−4 and Figure 5−5).

Table 5−5. Reset, x_BIO, and Interrupt Timing Requirements

		MIN	MAX	UNIT
$t_{h(RS)}$	Hold time, x_RS after CLKOUT low	0		ns
$t_{h(BIO)}$	Hold time, x_BIO after CLKOUT low	0		ns
$t_{h(INT)}$	Hold time, x_INT, x_NMI, after CLKOUT low†	0		ns
$t_{w(RSL)}$	Pulse duration, x_RS low‡§	4H+4		ns
$t_{w(BIO)}$	Pulse duration, x_BIO low, synchronous†	5H		ns
$t_{w(INTH)}$	Pulse duration, x_INT, x_NMI high (synchronous)†	4H		ns
$t_{w(INTL)}$	Pulse duration, x_INT, x_NMI low (synchronous)†	4H		ns
$t_{w(INTL)WKP}$	Pulse duration, x_INT, x_NMI low for IDLE2/IDLE3 wakeup†	6		ns
$t_{su(RS)}$	Setup time, x_RS before CLKIN low§	4		ns
$t_{su(BIO)}$	Setup time, x_BIO before CLKOUT low	7		ns
$t_{su(INT)}$	Setup time, x_INT, x_NMI, x_RS before CLKOUT low	7		ns

† The external interrupts (x_INT, x_NMI) are synchronized to the core CPU by way of a two flip-flop synchronizer, which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1-0-0 sequence at the timing that is corresponding to a three-CLKOUT sampling sequence.

‡ If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, x_RS must be held low for at least 50 µs to ensure synchronization and lock-in of the PLL.

§ x_RS can cause a change in clock frequency, changing the value of H (see Section 3.2.6).

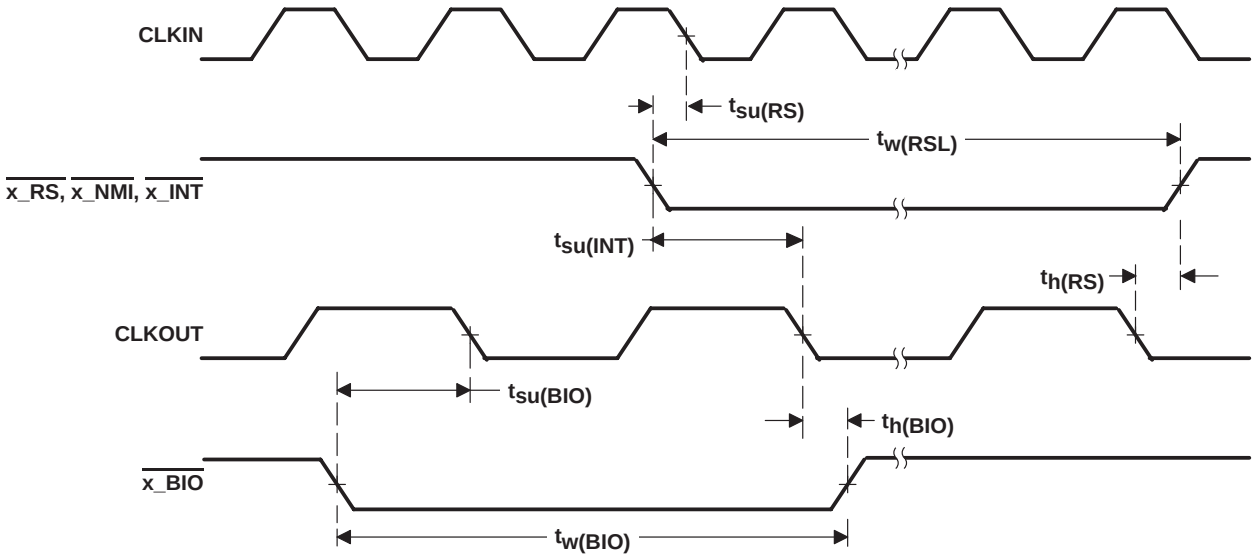


Figure 5−4. Reset and x_BIO Timings

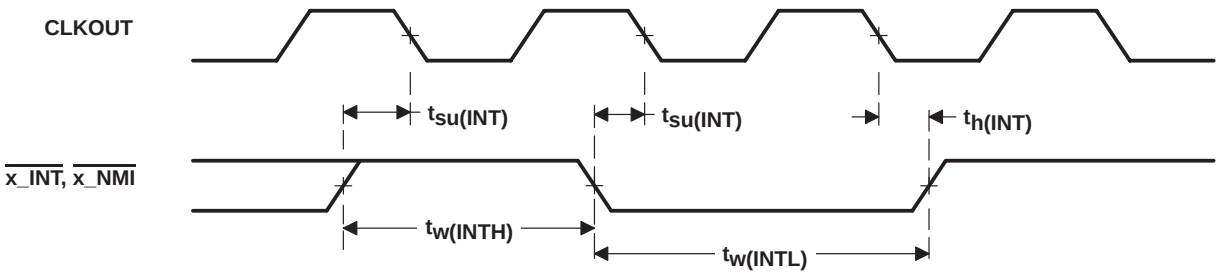


Figure 5−5. Interrupt Timing

5.7 External Flag (x_XF), Timer (x_TOUT), and Watchdog Timer Output ($\overline{\text{x\_WTOUT}}$) Timings

Table 5−6 assumes testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−6, Figure 5−7, and Figure 5−8).

Table 5−6. External Flag (x_XF), Timer (x_TOUT), and Watchdog Timer Output ($\overline{\text{x\_WTOUT}}$) Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(XF)}$	Delay time, CLKOUT high to x_XF high	− 1	4	ns
	Delay time, CLKOUT high to x_XF low	− 1	6	
$t_{d(TOUTH)}$	Delay time, CLKOUT high to x_TOUT high	− 1	4	ns
$t_{d(TOUTL)}$	Delay time, CLKOUT high to x_TOUT low	− 1	6	ns
$t_{w(TOUT)}$	Pulse duration, x_TOUT	2H −8	2H	ns
$t_{d(WTOUTH)}$	Delay time, CLKOUT high to $\overline{\text{x\_WTOUT}}$ high	− 1	4	ns
$t_{d(WTOUTL)}$	Delay time, CLKOUT high to $\overline{\text{x\_WTOUT}}$ low	− 1	4	ns
$t_{w(WTOUT)}$	Pulse duration, $\overline{\text{x\_WTOUT}}$	2H − 8		ns

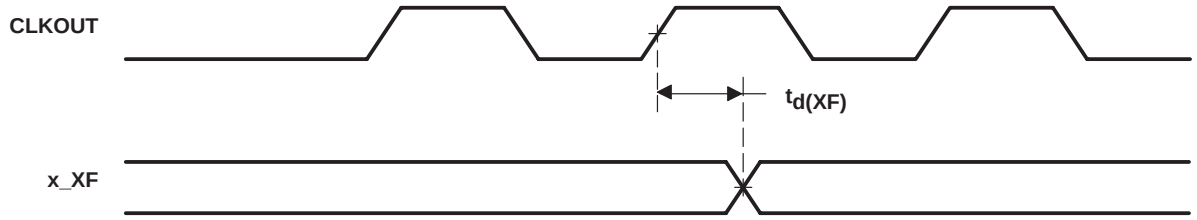


Figure 5−6. External Flag (x_XF) Timing

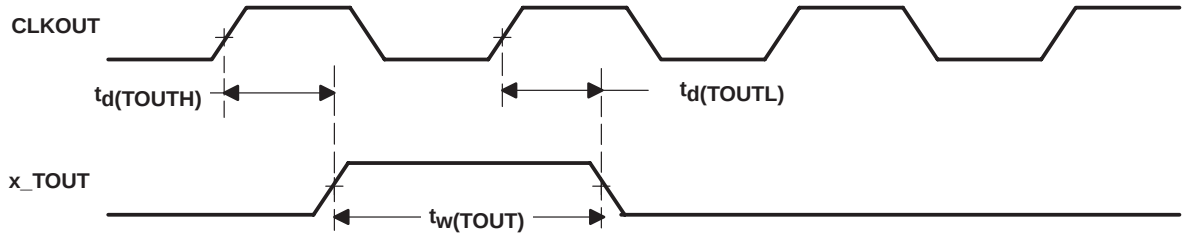


Figure 5−7. Timer (x_TOUT) Timing

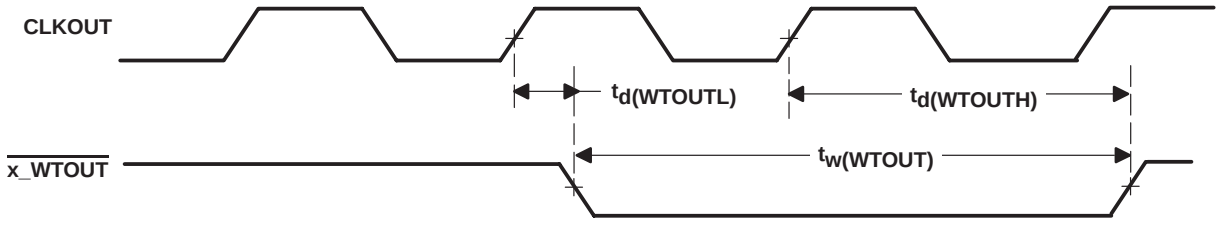


Figure 5−8. Watchdog Timer ($\overline{\text{x\_WTOUT}}$) Timing

5.8 General-Purpose Input/Output (GPIO) Timing

Table 5−7 and Table 5−8 assume testing over recommended operating conditions (see Figure 5−9).

Table 5−7. GPIO Timing Requirements

		MIN	MAX	UNIT
$t_{su(GPIO-COH)}$	Setup time, x_GPIOn input valid before CLKOUT high, x_GPIOn configured as general-purpose input.	8		ns
$t_{h(GPIO-COH)}$	Hold time, x_GPIOn input valid after CLKOUT high, x_GPIOn configured as general-purpose input.	0		ns

Table 5−8. GPIO Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(COH-GPIO)}$	Delay time, CLKOUT high to x_GPIOn output change. x_GPIOn configured as general-purpose output.	0	6	ns

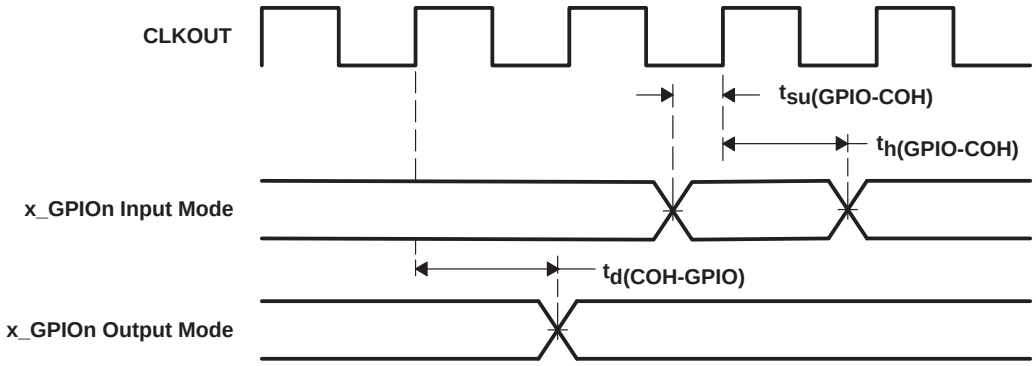


Figure 5−9. GPIO Timings

5.9 Multichannel Buffered Serial Port Timing

5.9.1 McBSP0/1/2 Transmit and Receive Timings

The serial port timings that are referenced to CLKOUT are actually related to the internal CPU clock frequency. These timings are not affected by the value of the DIVFCT bit field in the BSCR register (see Section 3.2.2.5 of this data manual for details on the BSCR register). Any references to CLKOUT in these timing parameters refer to the CLKOUT timings when no divide factor is selected (DIVFCT = 00b).

Table 5−9 and Table 5−10 assume testing over recommended operating conditions and H = $0.5t_{c(CO)}$ (see Figure 5−10 and Figure 5−11).

Table 5−9. McBSP0/1/2 Transmit and Receive Timing Requirements†

			MIN	MAX	UNIT
$t_{c(BCKRX)}$	Cycle time, x_BCLKR/X	BCLKR/X ext	50		ns
$t_{w(BCKRX)}$	Pulse duration, x_BCLKR/X low or x_BCLKR/X high	BCLKR/X ext	24		ns
$t_{h(BCKRL-BFRH)}$	Hold time, external x_BFSR high after x_BCLKR low	BCLKR ext	7.5		ns
$t_{h(BCKRL-BDRV)}$	Hold time, x_BDR valid after x_BCLKR low	BCLKR ext	7.5		ns
$t_{h(BCKXL-BFXH)}$	Hold time, external x_BFSX high after x_BCLKX low	BCLKX ext	7.5		ns
$t_{su(BFRH-BCKRL)}$	Setup time, external x_BFSR high before x_BCLKR low	BCLKR ext	7.5		ns
$t_{su(BDRV-BCKRL)}$	Setup time, x_BDR valid before x_BCLKR low	BCLKR ext	7.5		ns
$t_{su(BFXH-BCKXL)}$	Setup time, external x_BFSX high before x_BCLKX low	BCLKX ext	7.5		ns
$t_{r(BCKRX)}$	Rise time, x_BCLKR/X	BCLKR/X ext		6	ns
$t_{f(BCKRX)}$	Fall time, x_BCLKR/X	BCLKR/X ext		6	ns

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

Table 5−10. McBSP0/1/2 Transmit and Receive Switching Characteristics†

PARAMETER				MIN	MAX	UNIT
$t_{d(BCKXH-BFXV)}$	Delay time, x_BCLKX high to internal x_BFSX valid		BCLKX ext	2	15	ns
$t_{dis(BCKXH-BDXHZ)}$	Disable time, x_BCLKX high to x_BDX high impedance following last data bit		BCLKX ext	1	18	ns
$t_{d(BCKXH-BDXV)}$	Delay time, x_BCLKX high to x_BDX valid. This applies to all bits except the first bit transmitted.		BCLKX ext	4	20	ns
	Delay time, x_BCLKX high to x_BDX valid.‡ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 0	BCLKX ext		16	
		DXENA = 1	BCLKX ext		4H+19	
$t_{en(BCKXH-BDX)}$	Enable time, x_BCLKX high to x_BDX driven.‡ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 0	BCLKX ext	2		ns
		DXENA = 1	BCLKX ext	4H+2		
$t_{d(BFXH-BDXV)}$	Delay time, x_BFSX high to x_BDX valid.‡ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 0	BFSX ext		17	ns
		DXENA = 1	BFSX ext		4H+15	
$t_{en(BFXH-BDX)}$	Enable time, x_BFSX high to x_BDX driven.‡ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 0	BFSX ext	1		ns
		DXENA = 1	BFSX ext	4H+5		

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ See the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for a description of the DX enable (DXENA) and data delay features of the McBSP.

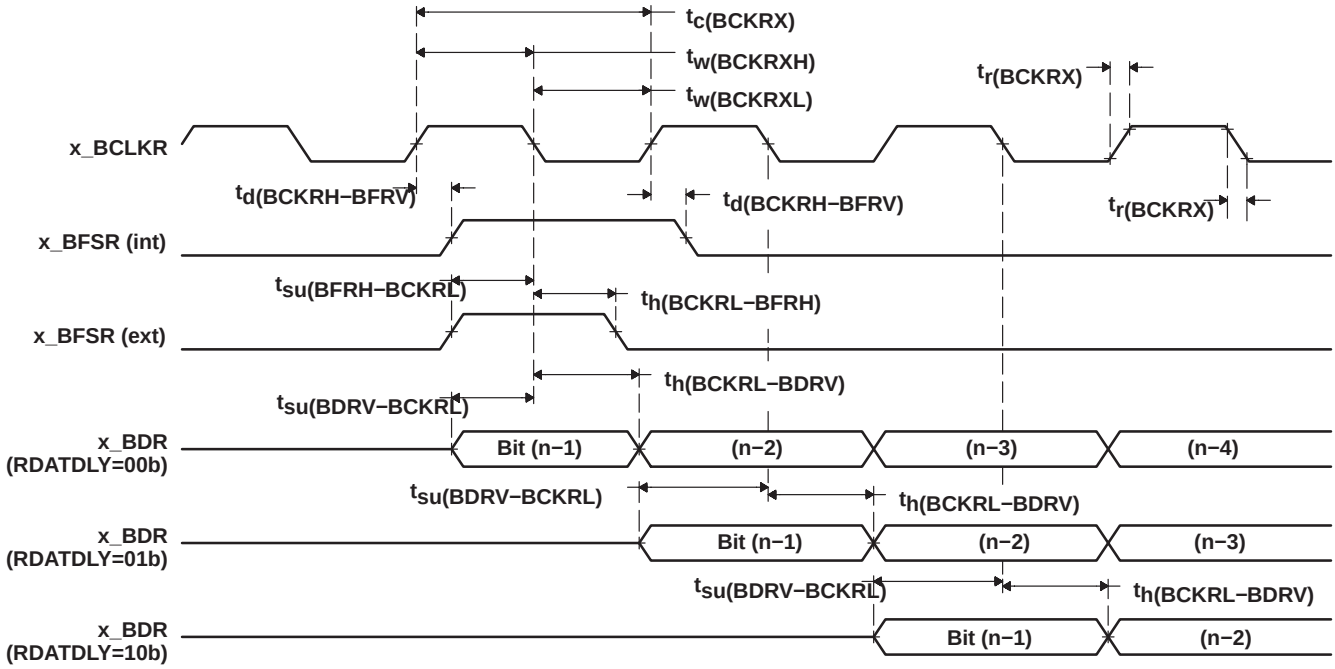


Figure 5−10. McBSP0/1/2 Receive Timings

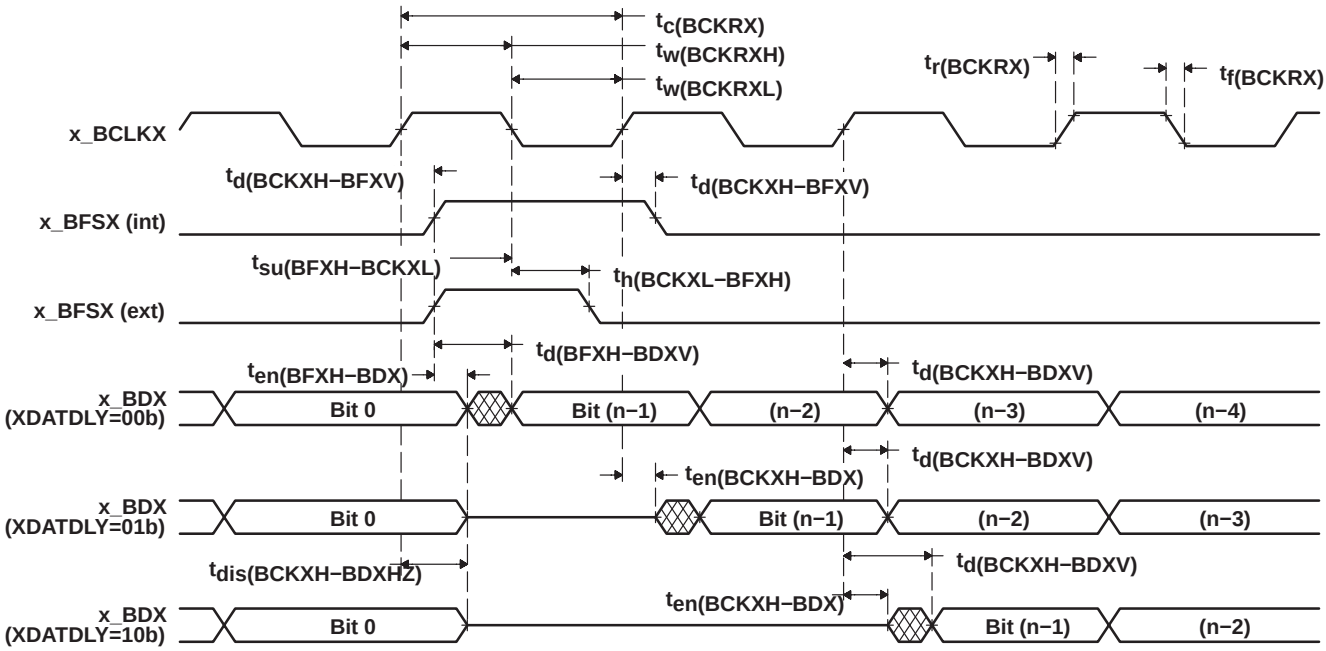


Figure 5−11. McBSP0/1/2 Transmit Timings

5.9.2 McBSP0 General-Purpose I/O Timing

Table 5−11 and Table 5−12 assume testing over recommended operating conditions (see Figure 5−12).

Table 5−11. McBSP0 General-Purpose I/O Timing Requirements

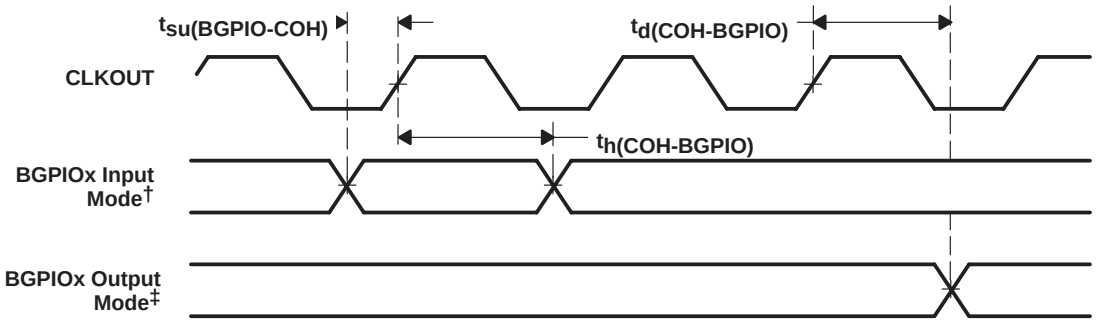
		MIN	MAX	UNIT
$t_{su(BGPIO-COH)}$	Setup time, BGPIOx input mode before CLKOUT high†	7		ns
$t_{h(COH-BGPIO)}$	Hold time, BGPIOx input mode after CLKOUT high†	0		ns

† BGPIOx refers to x_BCLKR, x_BFSR, x_BDR, x_BCLKX, or x_BFSX when configured as a general-purpose input.

Table 5−12. McBSP0 General-Purpose I/O Switching Characteristics

PARAMETER		MIN	MAX	UNIT
$t_{d(COH-BGPIO)}$	Delay time, CLKOUT high to BGPIOx output mode‡	−8	8	ns

‡ BGPIOx refers to x_BCLKR, x_BFSR, x_BCLKX, x_BFSX, or x_BDX when configured as a general-purpose output.



† BGPIOx refers to x_BCLKR, x_BFSR, x_BDR, x_BCLKX, or x_BFSX when configured as a general-purpose input.
‡ BGPIOx refers to x_BCLKR, x_BFSR, x_BCLKX, x_BFSX, or x_BDX when configured as a general-purpose output.

Figure 5−12. McBSP0 General-Purpose I/O Timings

5.10 Host-Port Interface (HPI16) Timing

Table 5−13 and Table 5−14 assume testing over recommended operating conditions and H = 0.5$t_{c(CO)}$ (see Figure 5−13 through Figure 5−19). In the following tables, DS refers to the logical OR of $\overline{HCS}$, $\overline{HDS1}$, and $\overline{HDS2}$, and HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.).

Table 5−13. HPI16 Timing Requirements

				MIN	MAX	UNIT
$t_{su(HBV-DSL)}$	Setup time, HAD valid before $\overline{DS}$ falling edge†‡			4		ns
$t_{h(DSL-HBV)}$	Hold time, HAD valid after $\overline{DS}$ falling edge†‡			4		ns
$t_{su(HBV-HSL)}$	Setup time, HAD valid before $\overline{HAS}$ falling edge†			4		ns
$t_{h(HSL-HBV)}$	Hold time, HAD valid after $\overline{HAS}$ falling edge†			4		ns
$t_{su(HAV-DSH)}$	Setup time, address valid before $\overline{DS}$ rising edge (nonmultiplexed write)‡			5		ns
$t_{su(HAV-DSL)}$	Setup time, address valid before $\overline{DS}$ falling edge (nonmultiplexed read)‡			−(4H + 5)		ns
$t_{h(DSH-HAV)}$	Hold time, address valid after $\overline{DS}$ rising edge (nonmultiplexed mode)‡			2		ns
$t_{su(HSL-DSL)}$	Setup time, $\overline{HAS}$ low before $\overline{DS}$ falling edge‡			4		ns
$t_{h(HSL-DSL)}$	Hold time, $\overline{HAS}$ low after $\overline{DS}$ falling edge‡			2		ns
$t_{w(DSL)}$	Pulse duration, $\overline{DS}$ low‡			23		ns
$t_{w(DSH)}$	Pulse duration, $\overline{DS}$ high‡			8		ns
$t_{c(DSH-DSH)}$	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge‡	Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with no DMA activity.	Reads	10H + 20		ns
			Writes	10H + 10		
		Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with 16-bit DMA activity.	Reads	16H + 20		ns
			Writes	16H + 10		
		Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with 32-bit DMA activity.	Reads	24H + 20		ns
			Writes	24H + 10		
	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge‡ (In autoincrement mode, WRITE timings are the same as READ timings.)	Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with no DMA activity.		10H + 10		ns
		Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with 16-bit DMA activity.		16H + 10		ns
		Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with 32-bit DMA activity.		24H + 10		ns
	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge for writes to DSPINT and $\overline{x\_HINT}$			8H		ns
	Cycle time, $\overline{DS}$ rising edge to next $\overline{DS}$ rising edge for HPIC reads, HPIC XADD bit writes, and address register reads and writes			40		ns
$t_{su(HDV-DSH)W}$	Setup time, HD valid before $\overline{DS}$ rising edge‡			4		ns
$t_{h(DSH-HDV)W}$	Hold time, HD valid after $\overline{DS}$ rising edge, write‡			2		ns
$t_{su(SELV-DSL)}$	Setup time, HPI_SEL1/SEL2 valid before $\overline{DS}$ falling edge‡			4		ns
$t_{h(DSH-SELV)}$	Hold time, HPI_SEL1/SEL2 valid after $\overline{DS}$ rising edge‡			1		ns

† HAD stands for HCNTL0, HCNTL1, and HR/$\overline{W}$.

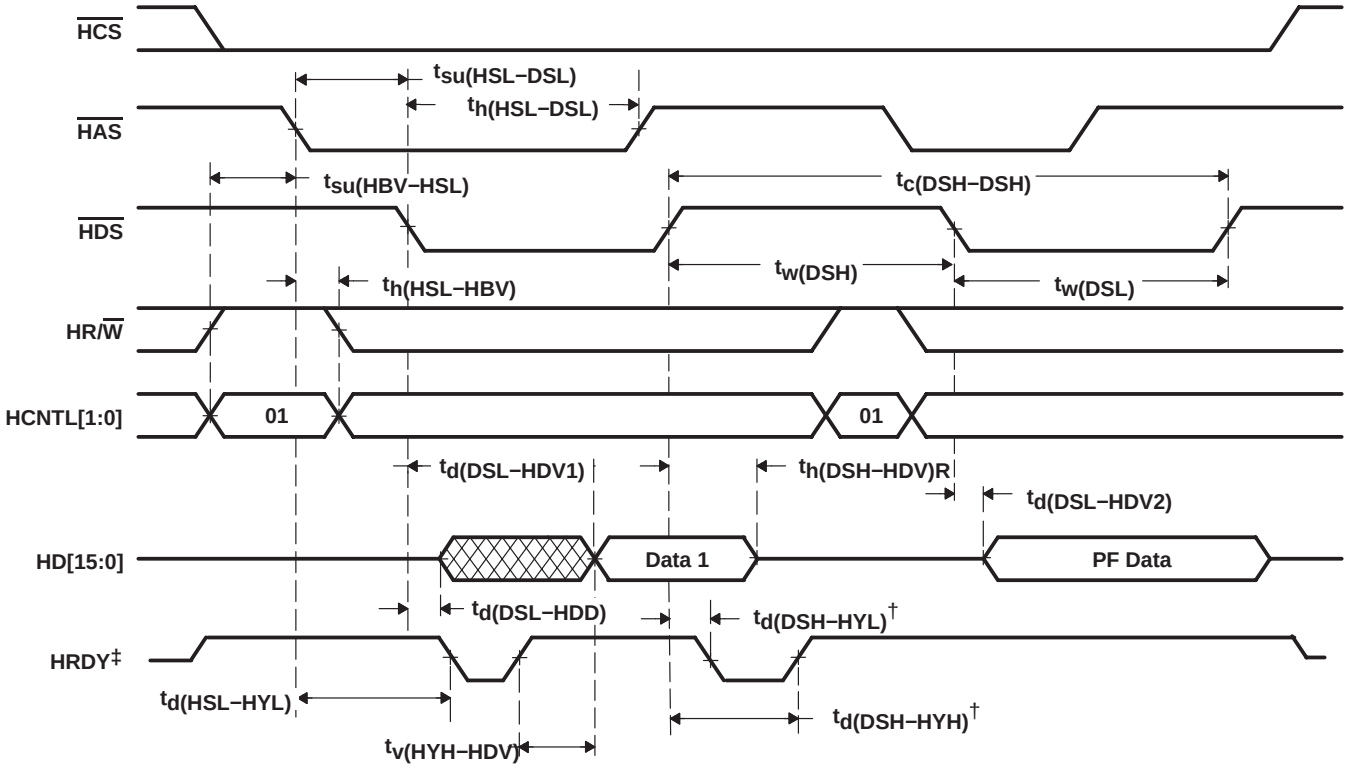
‡ $\overline{DS}$ refers to either $\overline{HCS}$ or $\overline{HDS}$, whichever is controlling the transfer. Refer to the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for information regarding logical operation of the HPI16. These timings are shown assuming that $\overline{HDS}$ is the signal controlling the transfer.

Table 5−14. HPI16 Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{d(DSL-HDD)}$	Delay time, $\overline{DS}$ low to HD driven†		3	20	ns
$t_{d(DSL-HDV1)}$	Delay time, $\overline{DS}$ low to HD valid for first word of an HPI read	Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 18H		32H+20 − $t_{w(DSH)}$	ns
		Case 1b: Memory accesses initiated by an autoincrement when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 18H		16H+20 − $t_{w(DSH)}$	ns
		Case 1c: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is active in 16-bit mode		16H+20	ns
		Case 1d: Memory accesses initiated by an autoincrement when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was ≥ 18H		20	
		Case 1e: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 26H		48H+20 − $t_{w(DSH)}$	ns
		Case 1f: Memory access initiated by an autoincrement when DMAC is active in 32-bit mode and $t_{w(DSH)}$ was < 26H		24H+20 − $t_{w(DSH)}$	ns
		Case 1g: Memory access not initiated by an autoincrement (or not immediately following a write) when DMAC is active in 32-bit mode		24H+20	
		Case 1h: Memory access initiated by an autoincrement when DMAC is active in 32-bit mode and $t_{w(DSH)}$ was ≥ 26H		20	
		Case 2a: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_{w(DSH)}$ was < 10H		20H+20 − $t_{w(DSH)}$	ns
		Case 2b: Memory accesses initiated by an autoincrement when DMAC is inactive and $t_{w(DSH)}$ was < 10H		10H+20 − $t_{w(DSH)}$	ns
		Case 2c: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is inactive		10H+20	
		Case 2d: Memory accesses initiated by an autoincrement when DMAC is inactive and $t_{w(DSH)}$ was ≥ 10H		20	
		Case 3: HPIC/HPIA reads		20	
$t_{d(DSL-HDV2)}$	Multiplexed reads with autoincrement. Prefetch completed.		3	20	ns
$t_{d(DSH-HYH)}$	Delay time, $\overline{DS}$ high to HRDY high† (writes and autoincrement reads)	Memory accesses (or writes to the FETCH bit) when no DMA is active		10H+5	ns
		Memory accesses (or writes to the FETCH bit) with one or more 16-bit DMA channels active		16H+5	
		Memory accesses (or writes to the FETCH bit) with one or more 32-bit DMA channels active		24H+5	
		Writes to DSPINT and $\overline{x\_HINT}$‡		4H + 5	
$t_{v(HYH-HDV)}$	Valid time, HD valid after HRDY high			6	ns
$t_{h(DSH-HDV)R}$	Hold time, HD valid after $\overline{DS}$ rising edge, read†		0	10	ns
$t_{d(DSL-HYL)}$	Delay time, $\overline{DS}$ low to HRDY low†			18	ns
$t_{d(DSH-HYL)}$	Delay time, $\overline{DS}$ high to HRDY low†			18	ns
$t_{d(HSL-HYL)}$	Delay time, $\overline{HAS}$ low to HRDY low, read			18	ns

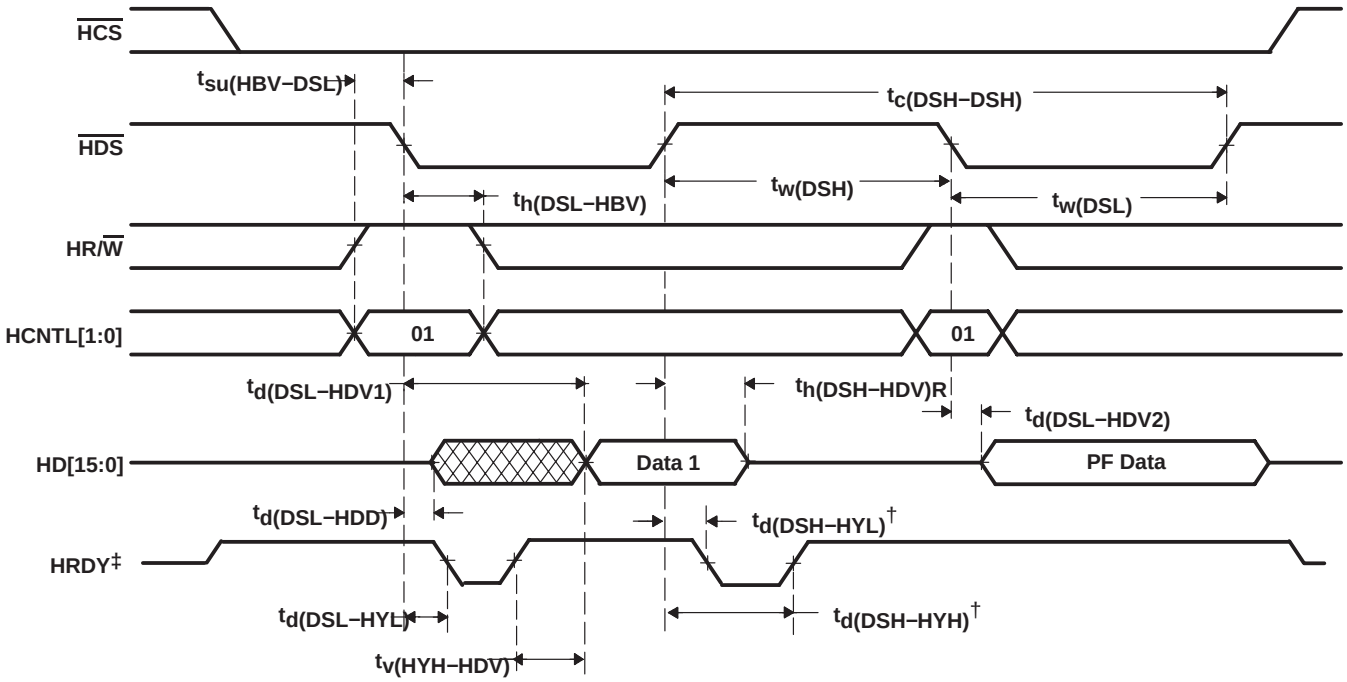
† $\overline{DS}$ refers to either $\overline{HCS}$ or $\overline{HDS}$, whichever is controlling the transfer. Refer to the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for information regarding logical operation of the HPI16. These timings are shown assuming that $\overline{HDS}$ is the signal controlling the transfer.

‡ HRDY does not go low for other register accesses.



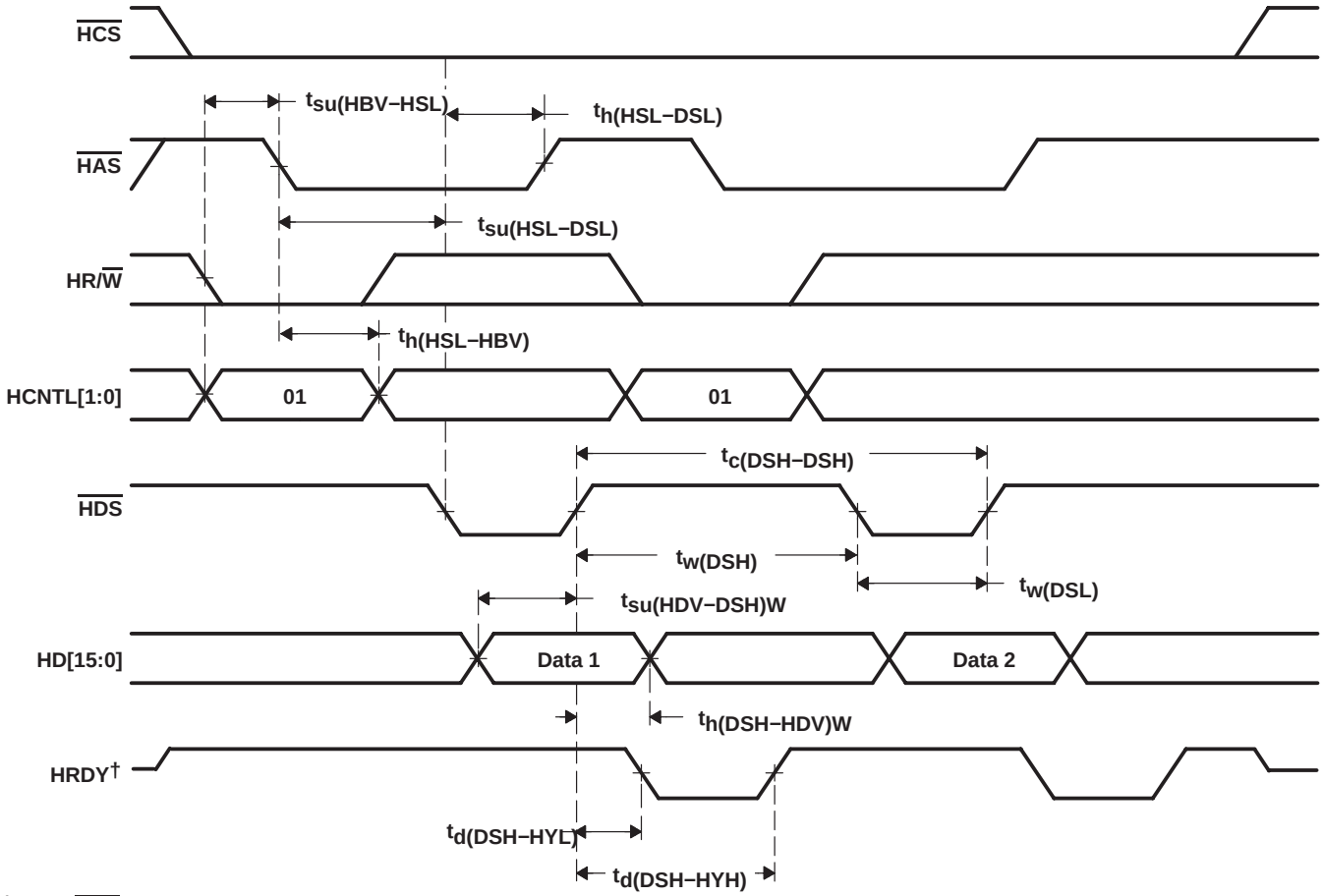
† HRDY goes low at these times only after autoincrement reads.
‡ While $\overline{\text{HCS}}$ is not selected, HRDY is in high-Z state.

Figure 5−13. Multiplexed Read Timings Using $\overline{\text{HAS}}$



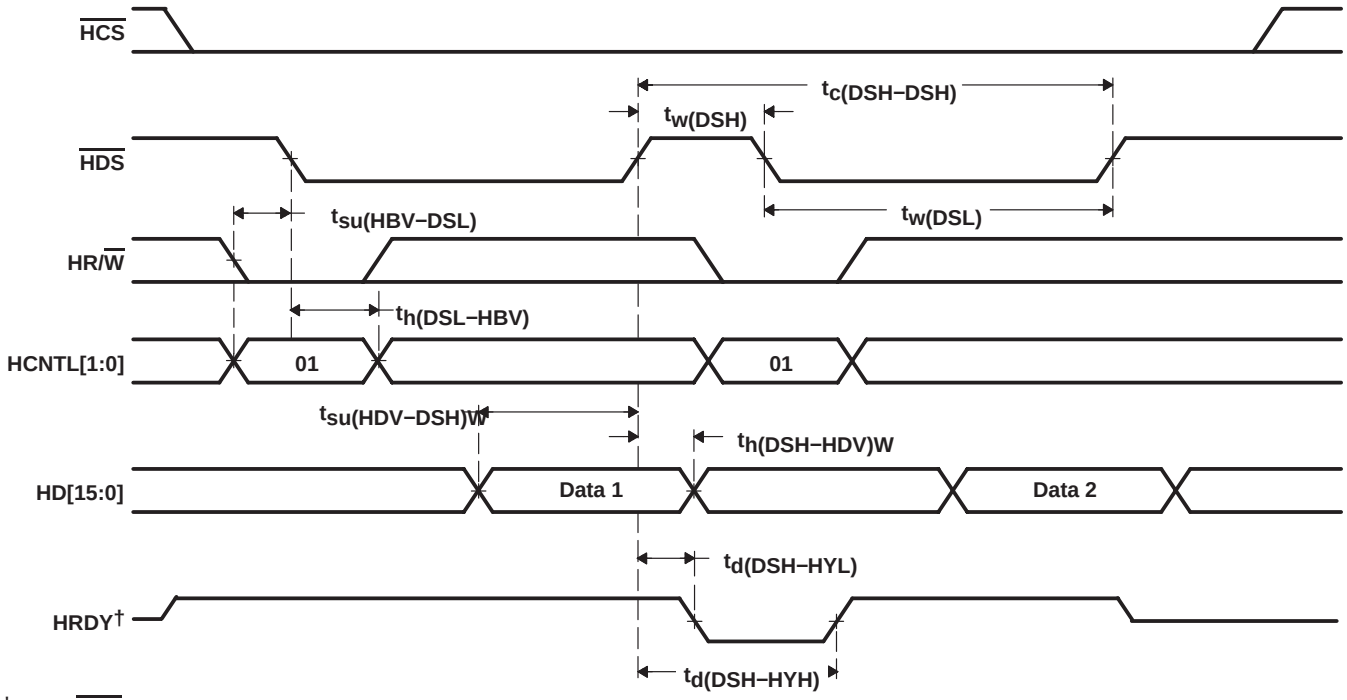
† HRDY goes low at these times only after autoincrement reads.
‡ While HCS is not selected, HRDY is in high-Z state.

Figure 5−14. Multiplexed Read Timings With HAS Held High



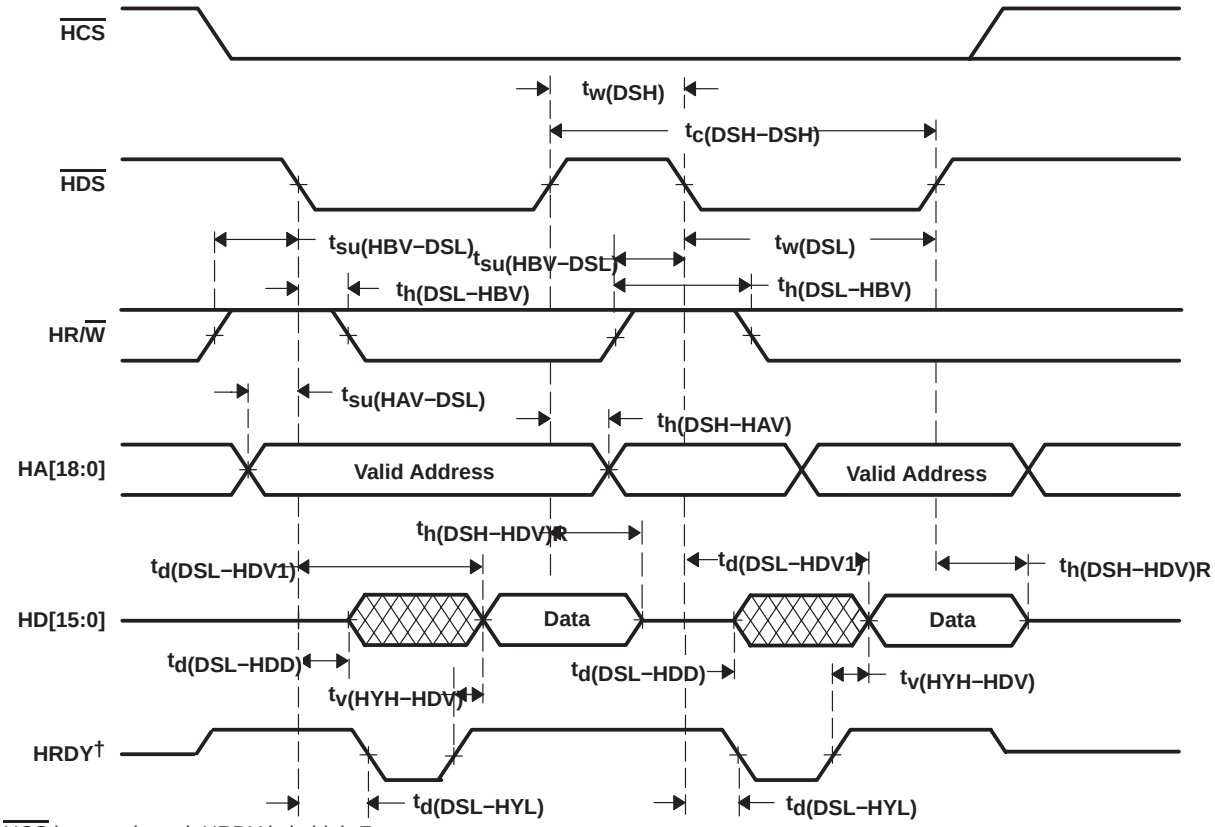
† While $\overline{\text{HCS}}$ is not selected, HRDY is in high-Z state.

Figure 5−15. Multiplexed Write Timings Using $\overline{\text{HAS}}$



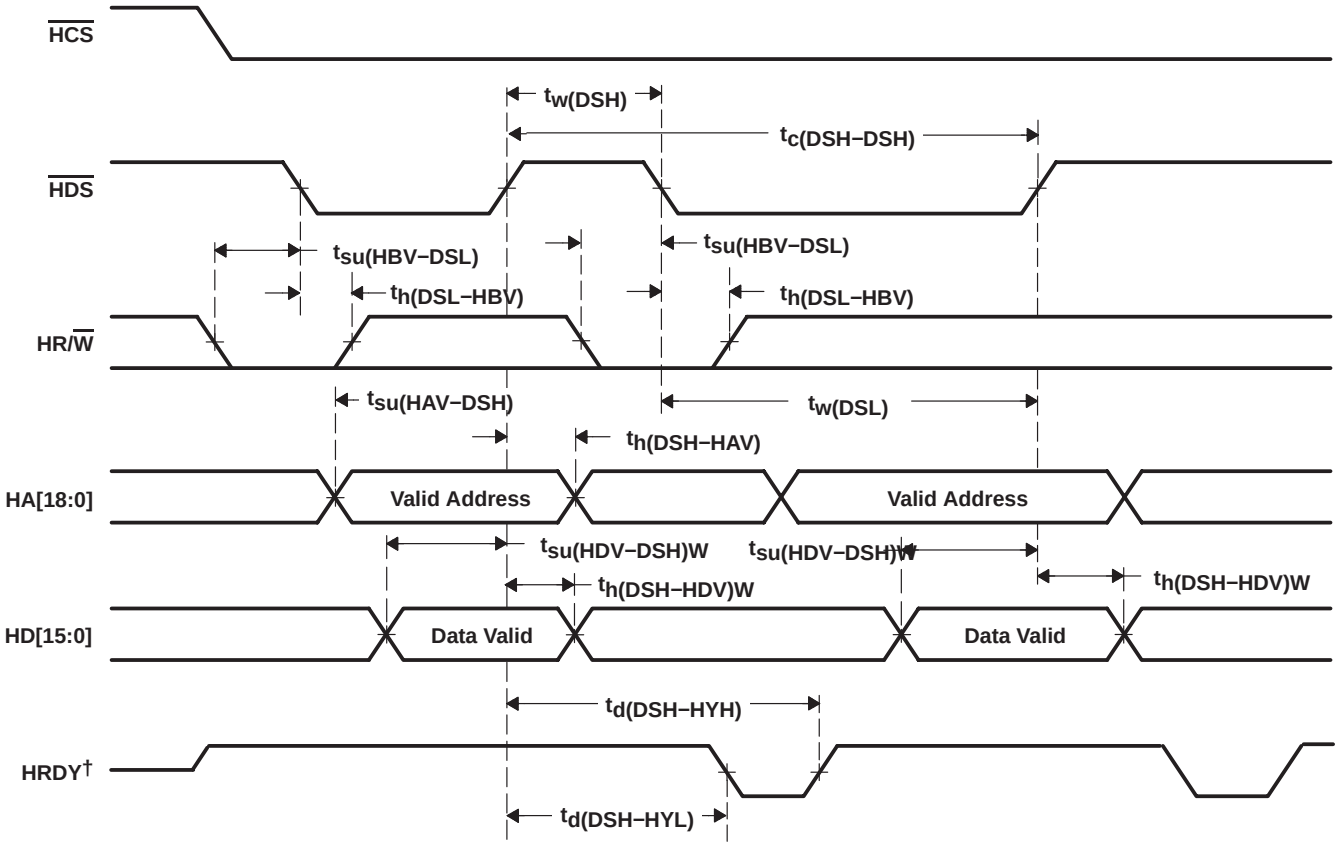
† While $\overline{\text{HCS}}$ is not selected, HRDY is in high-Z state.

Figure 5−16. Multiplexed Write Timings With $\overline{\text{HAS}}$ Held High



† While $\overline{HCS}$ is not selected, HRDY is in high-Z state.

Figure 5−17. Nonmultiplexed Read Timings



† While $\overline{\text{HCS}}$ is not selected, HRDY is in high-Z state.

Figure 5−18. Nonmultiplexed Write Timings

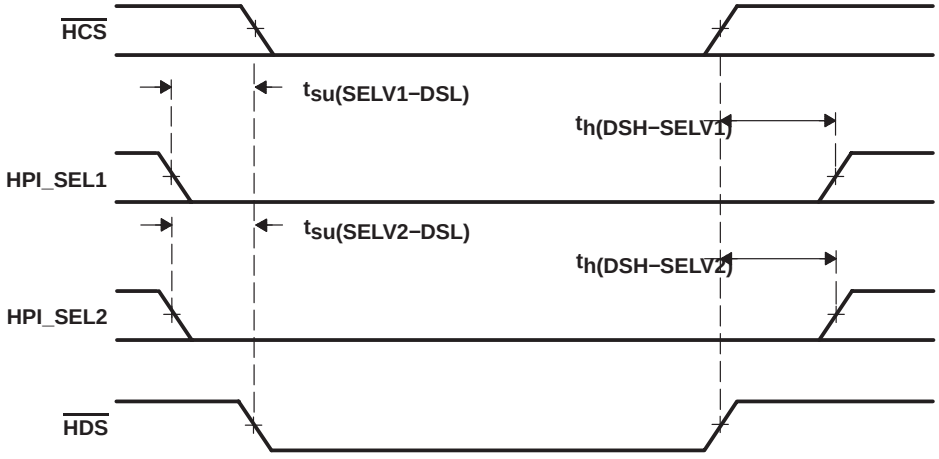


Figure 5−19. HPI_SEL1 and HPI_SEL2 Timing

6 Mechanical Data

6.1 Package Thermal Resistance Characteristics

Table 6−1 provides the thermal resistance characteristics for the recommended package types used on the TMS320VC5441 DSP.

Table 6−1. Thermal Resistance Characteristics

PARAMETER	GGU PACKAGE	PGF PACKAGE	UNIT
$R_{\Theta JA}$	38	56	°C/W
$R_{\Theta JC}$	5	5	°C/W

6.2 Packaging Information

The following packaging information reflects the most current released data available for the designated device(s). This data is subject to change without notice and without revision of this document.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320VC5441AGGU	ACTIVE	BGA MICROSTAR	GGU	169	160	TBD	SNPB	Level-3-220C-168 HR	-40 to 100	DVC5441AGGU	Samples
TMS320VC5441APGF	ACTIVE	LQFP	PGF	176	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 100	320VC5441APGF TMS	Samples
TMS320VC5441AZGU	ACTIVE	BGA MICROSTAR	ZGU	169	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 100	DVC5441AZGU	Samples
TMS320VC5441AZGUZE	ACTIVE	BGA MICROSTAR	ZGU	169	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 100	DVC5441AZGU	Samples
TMS320VC5441GGU	ACTIVE	BGA MICROSTAR	GGU	169	160	TBD	SNPB	Level-3-220C-168 HR	0 to 85	DVC5441GGU	Samples
TMS320VC5441PGF	ACTIVE	LQFP	PGF	176	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 85	320VC5441PGF TMS	Samples
TMS320VC5441ZGU	ACTIVE	BGA MICROSTAR	ZGU	169	160	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	0 to 85	DVC5441ZGU	Samples
TNETV2842VNDGGU	ACTIVE	BGA MICROSTAR	GGU	169	160	TBD	SNPB	Level-3-220C-168 HR	0 to 85	DVC5441GGU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

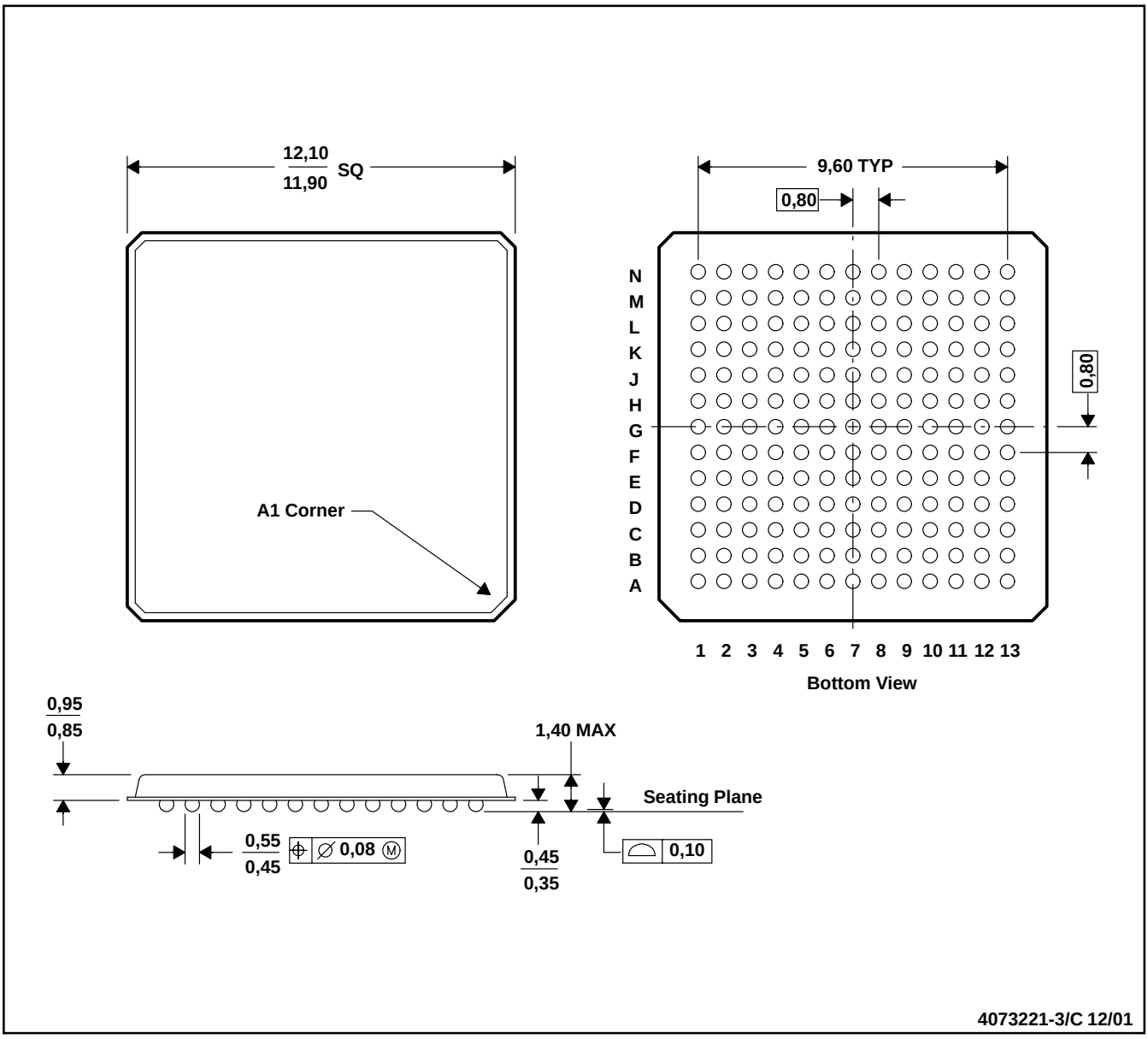
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

MPBG157A – AUGUST 2000 – REVISED MAY 2002

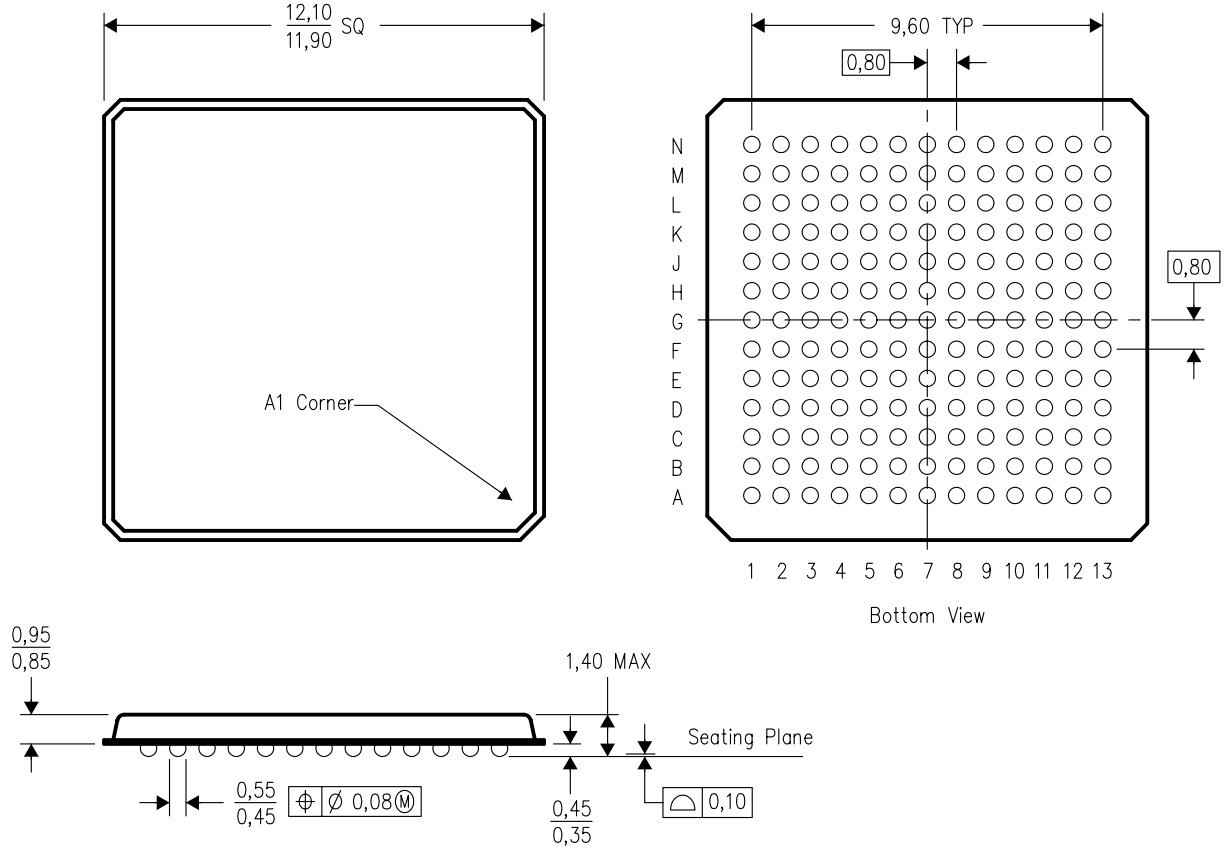
GGU (S–PBGA–N169) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

MicroStar BGA is a trademark of Texas Instruments Incorporated.

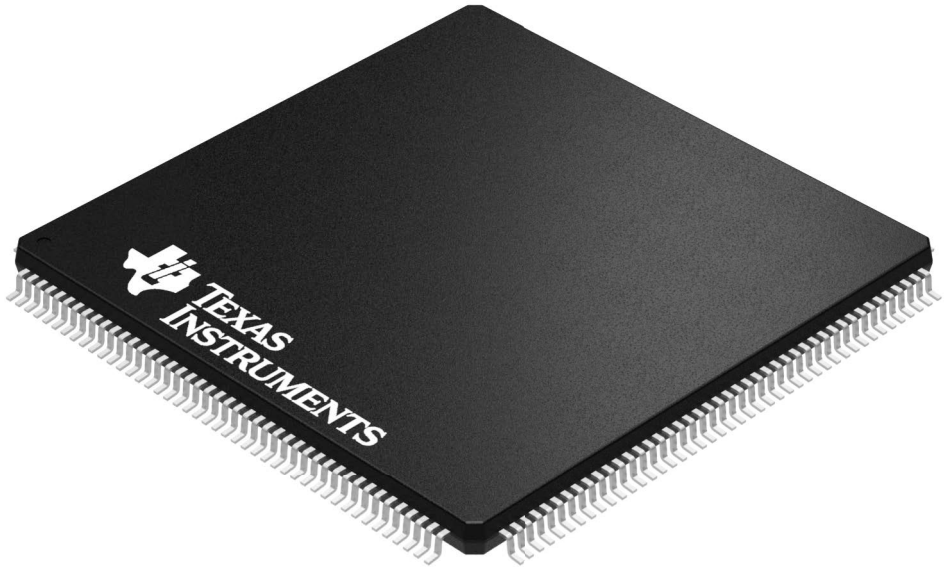
ZGU (S–PBGA–N169) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Micro Star BGA configuration
D. This is a lead–free solder ball design.

PGF 176 LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



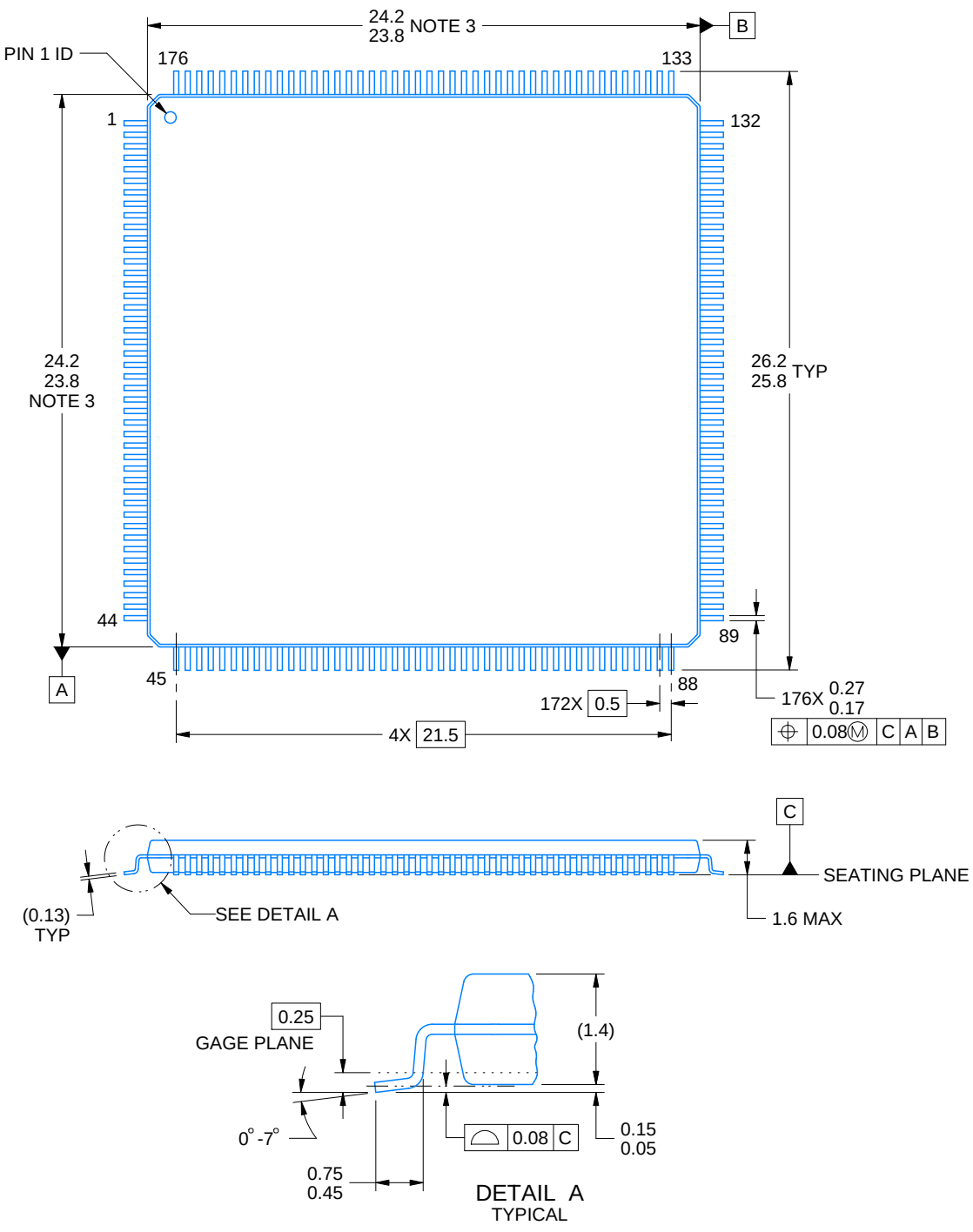
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PGF0176A

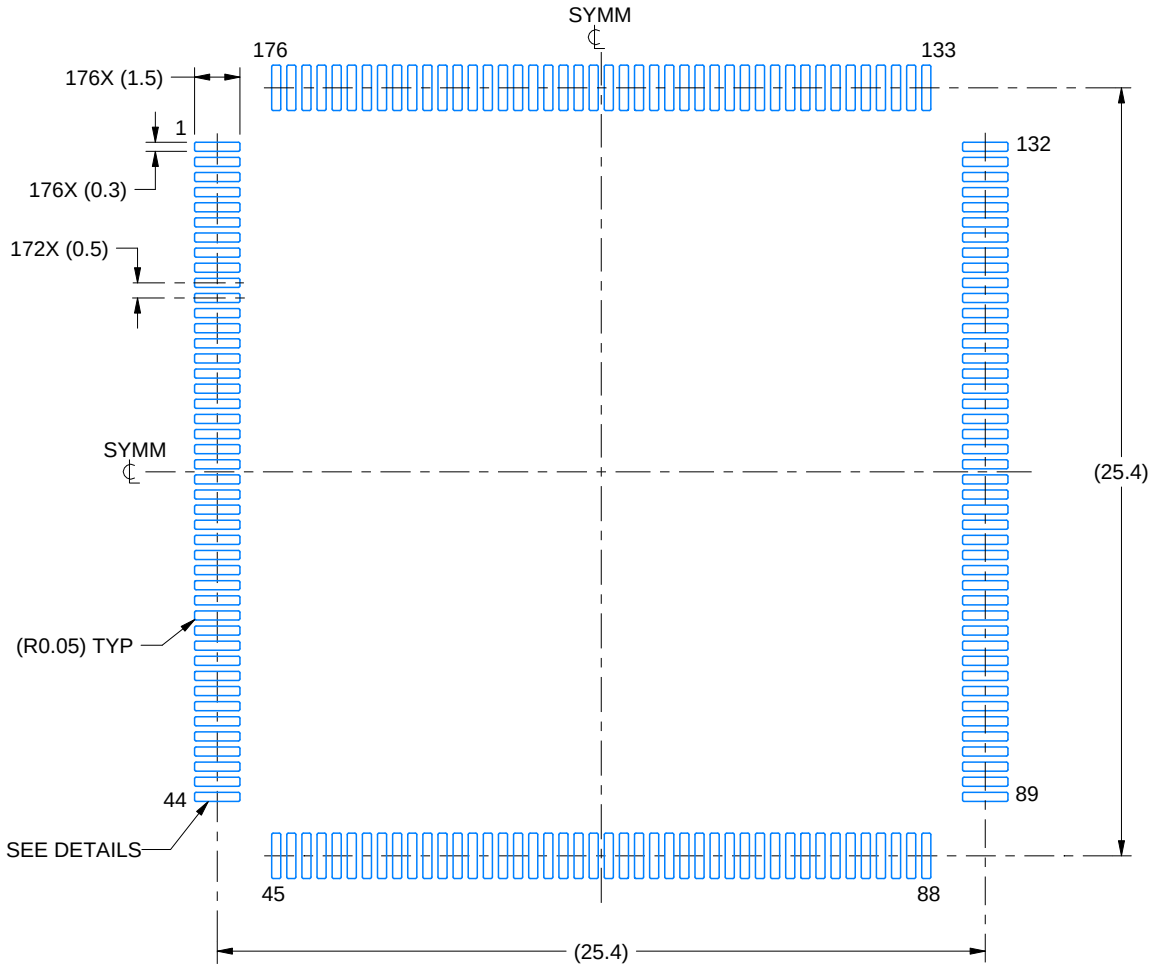
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

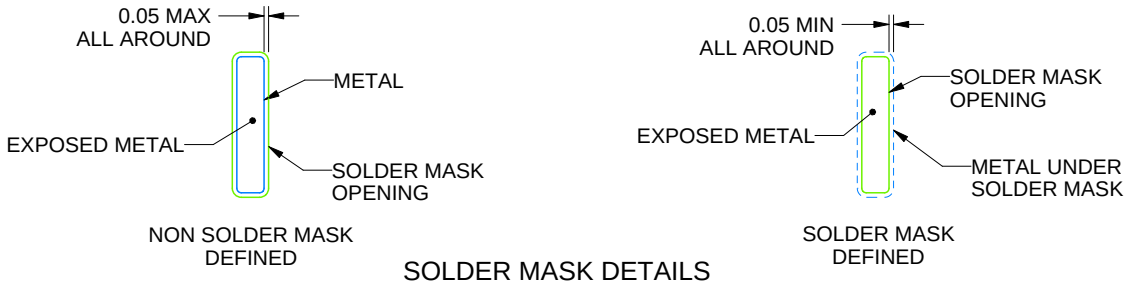


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:4X



SOLDER MASK DETAILS

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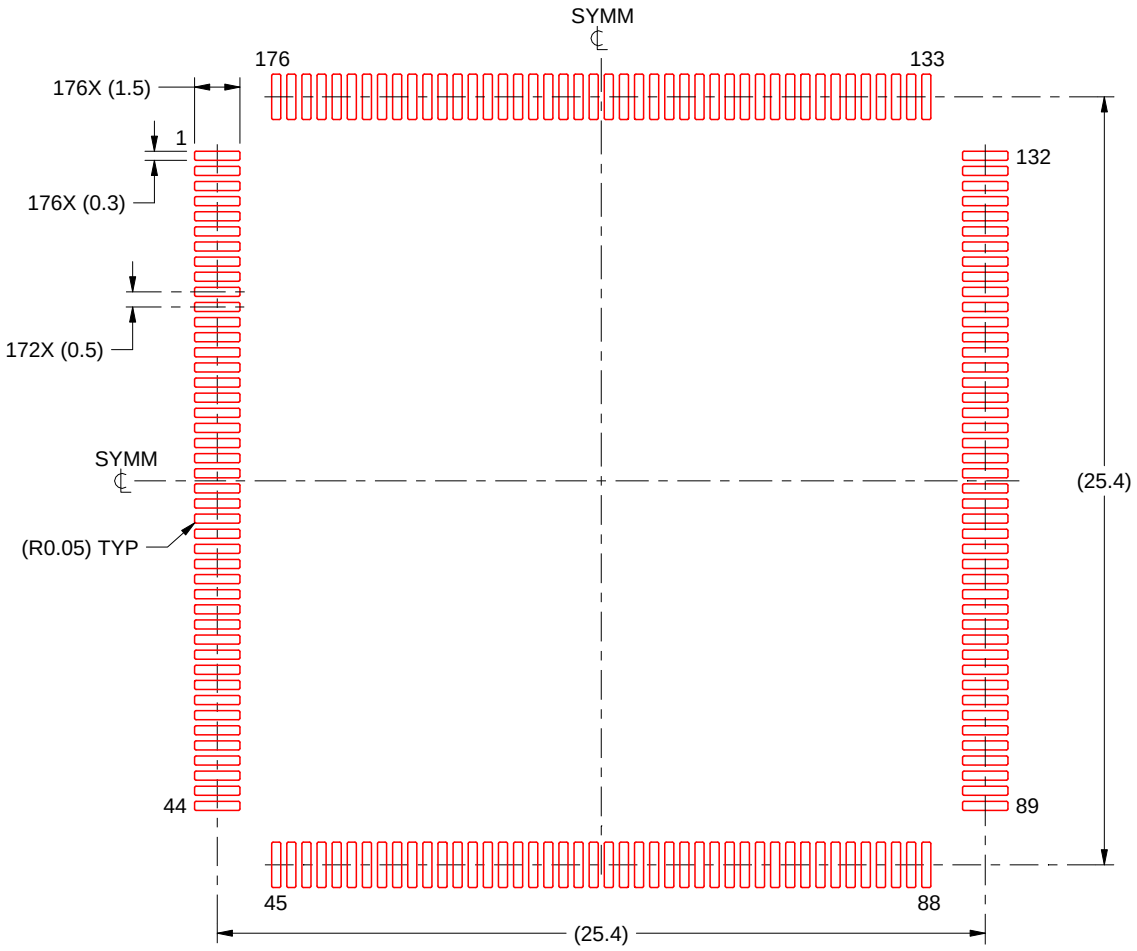
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4215177/A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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