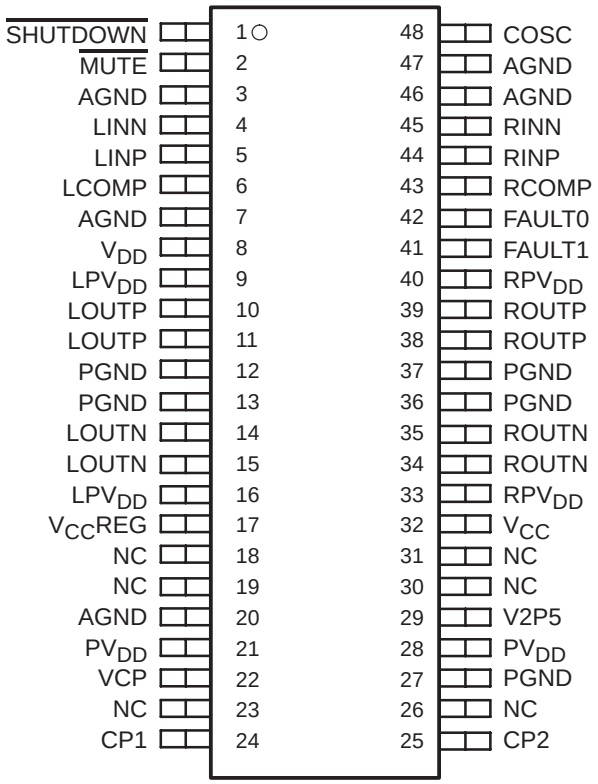
- **Extremely Efficient Class-D Stereo Operation**
- **Drives L and R Channels**
- **10-W BTL Output Into 4 Ω From 12 V**
- **32-W Peak Music Power**
- **Fully Specified for 12-V Operation**
- **Low Shutdown Current**
- **Thermally-Enhanced PowerPAD™ Surface-Mount Packaging**
- **Thermal and Under-Voltage Protection**

DCA PACKAGE
(TOP VIEW)



NC − No internal connection

description

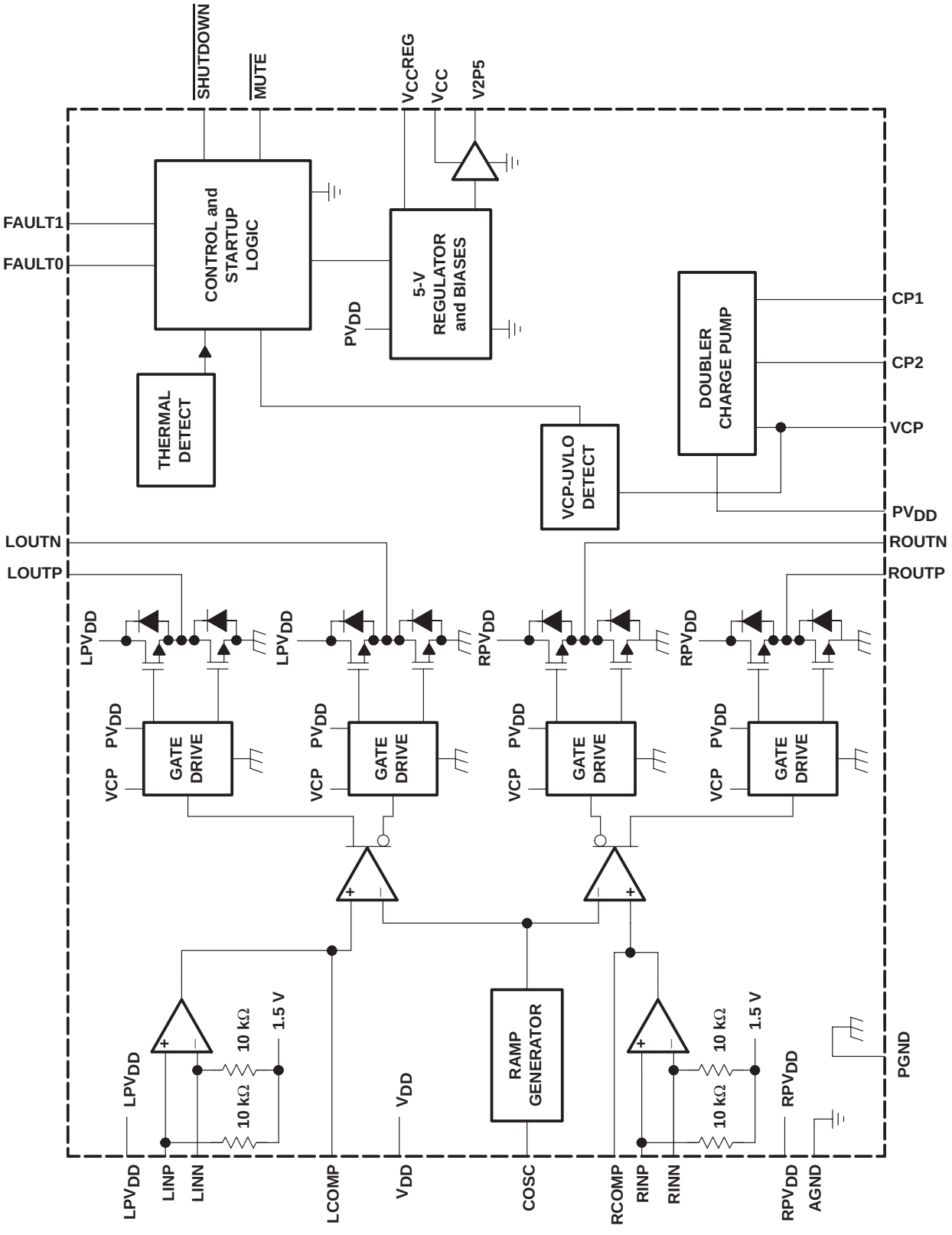
The TPA032D02 is a monolithic power IC stereo audio amplifier that operates in extremely efficient Class-D operation, using the high switching speed of power DMOS transistors to replicate the analog input signal through high-frequency switching of the output stage. This allows the TPA032D02 to be configured as a bridge-tied load (BTL) amplifier capable of delivering up to 10 W of continuous average power into a 4-Ω load at 0.5% THD+N from a 12-V power supply in the high-fidelity audio frequency range (20 Hz to 20 kHz). A BTL configuration eliminates the need for external coupling capacitors on the output. A chip-level shutdown control is provided to limit total supply current to 20 μA, making the device ideal for battery-powered applications.

The output stage is compatible with a range of power supplies from 8 V to 14 V. Protection circuitry is included to increase device reliability: thermal and under-voltage shutdown, with a status feedback terminal for use when any error condition is encountered.

The high switching frequency of the TPA032D02 allows the output filter to consist of three small capacitors and two small inductors per channel. The high switching frequency also allows for good THD+N performance.

The TPA032D02 is offered in the thermally enhanced 48-pin PowerPAD™ TSSOP surface-mount package (designator DCA).

schematic



NOTE A: LPV_{DD}, RPV_{DD}, and PV_{DD} are externally connected. AGND and PGND are externally connected.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
AGND	3, 7, 20, 46, 47	Analog ground for Class-D analog circuitry
COSC	48	Connect a capacitor from analog ground to this terminal to set the frequency of the ramp reference signal.
CP1	24	First diode node for charge pump
CP2	25	First inverter switching node for charge pump
FAULT0	42	Logic level fault0 output signal. Lower order bit of the two fault signals with open drain output.
FAULT1	41	Logic level fault1 output signal. Higher order bit of the two fault signals with open drain output.
LCOMP	6	Compensation capacitor terminal for left-channel Class-D amplifier
LINN	4	Class-D left-channel negative input
LINP	5	Class-D left-channel positive input
LOUTN	14, 15	Class-D amplifier left-channel negative output of H-bridge
LOUTP	10, 11	Class-D amplifier left-channel positive output of H-bridge
LPV_{DD}	9, 16	Class-D amplifier left-channel power supply
$\overline{MUTE}$	2	Active-low TTL logic-level mute input signal. When $\overline{MUTE}$ is held low, the selected amplifier is muted. When $\overline{MUTE}$ is held > high, the device operates normally. When the Class-D amplifier is muted, the low-side output transistors are turned on, shorting the load to ground.
NC	18, 19, 23, 26, 30, 31	No connection
PGND	12, 13	Power ground for left-channel H−bridge only
PGND	27	Power ground for charge pump only
PGND	36, 37	Power ground for right-channel H-bridge only
PV_{DD}	21, 28	V_{DD} supply for charge-pump and gate drive circuitry
RCOMP	43	Compensation capacitor terminal for right-channel Class-D amplifier
RINN	45	Class-D right-channel negative input
RINP	44	Class-D right-channel positive input
RPV_{DD}	33, 40	Class-D amplifier right-channel power supply
ROUTN	34, 35	Class-D amplifier right-channel negative output of H-bridge
ROUTP	38, 39	Class-D amplifier right-channel positive output of H-bridge
$\overline{SHUTDOWN}$	1	Active-low TTL logic-level shutdown input signal. When $\overline{SHUTDOWN}$ is held low, the device goes into shutdown mode. When $\overline{SHUTDOWN}$ is held high, the device operates normally.
V_{CC}	32	5V supply to logic. This terminal is typically connected to $V_{CC}REG$.
$V_{CC}REG$	17	5-V regulator output. This terminal requires a 1-μF capacitor to ground for stability reasons.
V2P5	29	2.5V internal reference bypass. This terminal requires a capacitor to ground.
VCP	22	Connect a capacitor from this terminal to power ground to provide storage for the charge pump output voltage.
V_{DD}	8	V_{DD} bias supply for analog circuitry. This terminal needs to be well filtered to prevent degrading the device performance.

Class-D amplifier faults

Table 1. Class-D Amplifier Fault Table

FAULT 0	FAULT 1	DESCRIPTION
1	1	No fault. The device is operating normally.
0	1	Charge pump under-voltage lock-out (VCP-UV) fault. All low-side transistors are turned on, shorting the load to ground. Once the charge pump voltage is restored, normal operation resumes, but FAULT1 is still active. This is not a latched fault, however. FAULT1 is cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.
0	0	Thermal fault. All the low-side transistors are turned on, shorting the load to ground. Once the junction temperature drops 20°C, normal operation resumes (not a latched fault). But the FAULTx terminals are still set and are cleared by cycling $\overline{\text{MUTE}}$, $\overline{\text{SHUTDOWN}}$, or the power supply.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP† (DCA)
−40°C to 125°C	TPA032D02DCA

† The DCA package is available in left-ended tape and reel. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA032D02DCAR).

absolute maximum ratings over operating free-air temperature range, T_C = 25°C (unless otherwise noted)†

Supply voltage, (V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}) . . . . . 14 V
Logic supply voltage, (V_{CC}) . . . . . 5.5 V
Input voltage, V_I ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$) . . . . . −0.3 V to 7 V
Output current, I_O (FAULT0, FAULT1), open drain terminated . . . . . 1 mA
Supply/load voltage, (FAULT0, FAULT1) . . . . . 7 V
Charge pump voltage, V_{CP} . . . . . PV_{DD} + 20 V
Continuous H-bridge output current (1 H-bridge conducting) . . . . . 3.5 A
Pulsed H-Bridge output current, each output, I_{max} (see Note 1) . . . . . 7 A
Continuous V_{CC}REG output current, I_O (V_{CC}REG) . . . . . 150 mA
Continuous total power dissipation, T_C = 25°C . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, T_J . . . . . −40°C to 150°C
Operating case temperature range, T_C . . . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle ≤ 2%

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$‡ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCA	5.6 W	44.8 mW/°C	3.6 W	2.9 W

‡ Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD™ package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}, PV_{DD}, LPV_{DD}, RPV_{DD}	8		14	V
Logic supply voltage, V_{CC}	4.5		5.5	V
High-level input voltage, V_{IH} ($\overline{MUTE}$, $\overline{SHUTDOWN}$)	2		V_{DD} + 0.3 V	V
Low-level input voltage, V_{IL} ($\overline{MUTE}$, $\overline{SHUTDOWN}$)	−0.3		0.8	V
Audio inputs, LINN, LINP, RINN, RINP, differential input voltage			1	V_{RMS}
PWM frequency	100	250	500	kHZ

electrical characteristics Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 4 Ω to 8 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power supply rejection ratio	V_{DD} = PV_{DD} = xPV_{DD} = 11 V to 13 V		−40		dB
I_{DD}	Supply current	No output filter connected		25	35	mA
$I_{DD(Mute)}$	Supply current, mute mode	$\overline{MUTE}$ = 0 V		10	18	mA
$I_{DD(S/D)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0 V		20	30	µA
$\|I_{IH}\|$	High-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IH} = 5.25 V			10	µA
$\|I_{IL}\|$	Low-level input current ($\overline{MUTE}$, MODE, $\overline{SHUTDOWN}$)	V_{IL} = −0.3 V			10	µA
$r_{DS(on)}$	Static drain-to-source on-state resistance (high-side + low-side FETs)	I_{DD} = 0.5 A		720	800	mΩ
$r_{DS(on)}$	Matching, high-side to high-side, low-side to low-side, same channel		95%	98%		

operating characteristics, Class-D amplifier, V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12 V, R_L = 4 Ω, T_A = 25°C, See Figure 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	f = 1 kHz, THD = 0.5%, per channel, Device soldered on PCB, See Note 2		10		W
	Efficiency	P_O = 10 W, f = 1 kHz		77%		
A_V	Gain			25		dB
	Left/right channel gain matching		92%	95%		
	Noise floor			−60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		−50		dB
	Frequency response bandwidth, post output filter, −3 dB		20		20000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, T_A = 23°C

operating characteristics, Class-D amplifier, $V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD} = 12$ V, $R_L = 8\ \Omega$, $T_A = 25°C$, See Figure 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power	THD = 0.5%, per channel, Device soldered on PCB, See Note 2		7.5		W
	Efficiency	P_O = 7.5 W, f = 1 kHz		85%		
A_V	Gain			25		dB
	Left/right channel gain matching		92%	95%		
	Noise floor			−60		dB
	Dynamic range			80		dB
	Crosstalk	f = 1 kHz		−50		dB
	Frequency response bandwidth, post output filter, −3 dB		20		20 000	Hz
B_{OM}	Maximum output power bandwidth				20	kHz
Z_I	Input impedance			10		kΩ

NOTE 2: Output power is thermally limited, $T_A = 85°C$

operating characteristics, V_{CC} 5-V regulator, $T_A = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD}$ = 8 V to 14 V, I_O = 0 to 90 mA	4.5		5.5	V
I_{OS}	Short-circuit output current	$V_{DD} = PV_{DD} = LPV_{DD} = RPV_{DD}$ = 8 V to 14 V†	90			mA

† Pulse width must be limited to prevent exceeding the maximum operating virtual junction temperature of 150°C.

thermal shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal shutdown temperature			165		°C
Thermal shutdown hysteresis			30		°C

PARAMETER MEASUREMENT INFORMATION

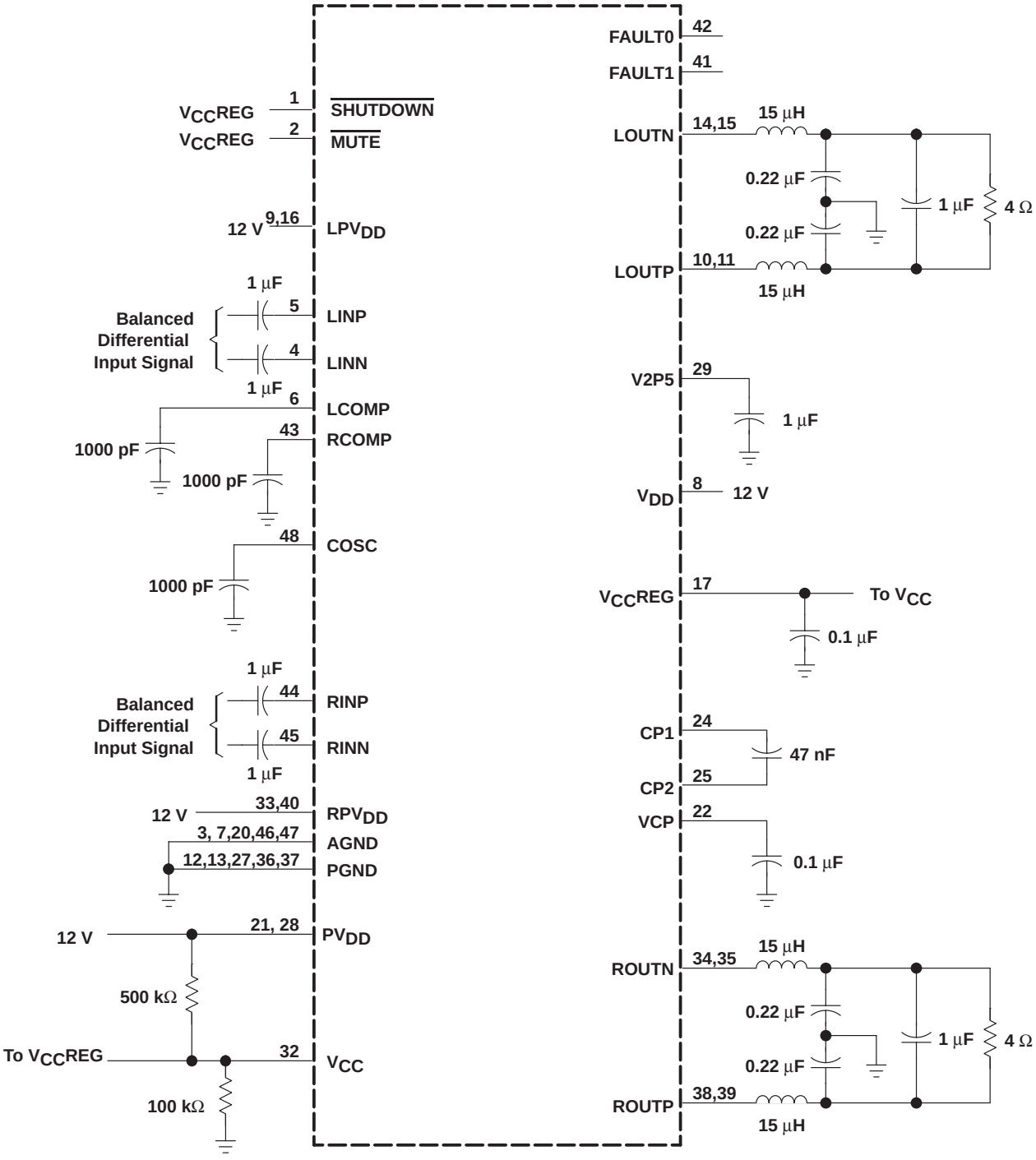


Figure 1. 12-V, 4-Ω Test Circuit

PARAMETER MEASUREMENT INFORMATION

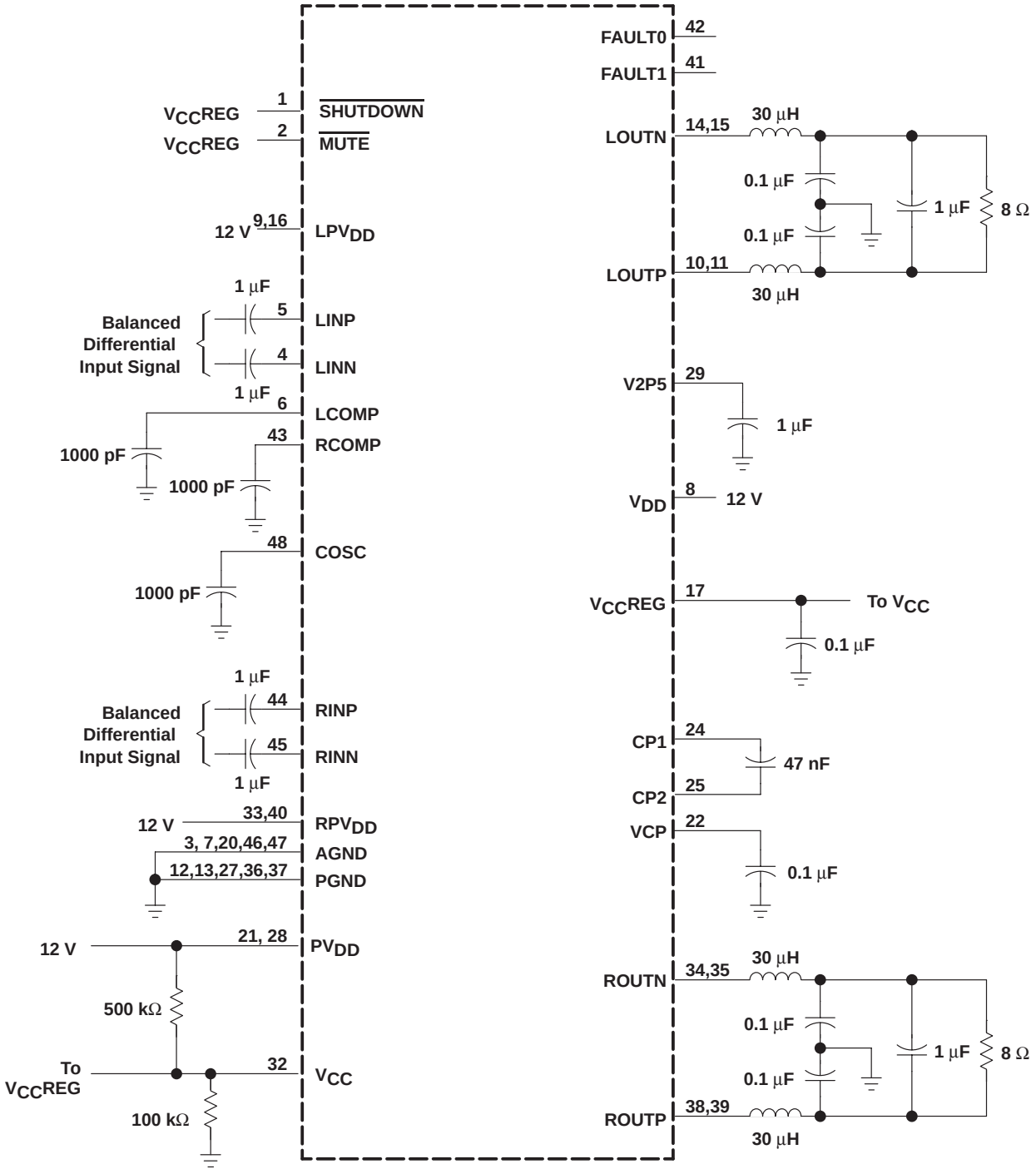


Figure 2. 12-V, 8-Ω Test Circuit

APPLICATION INFORMATION

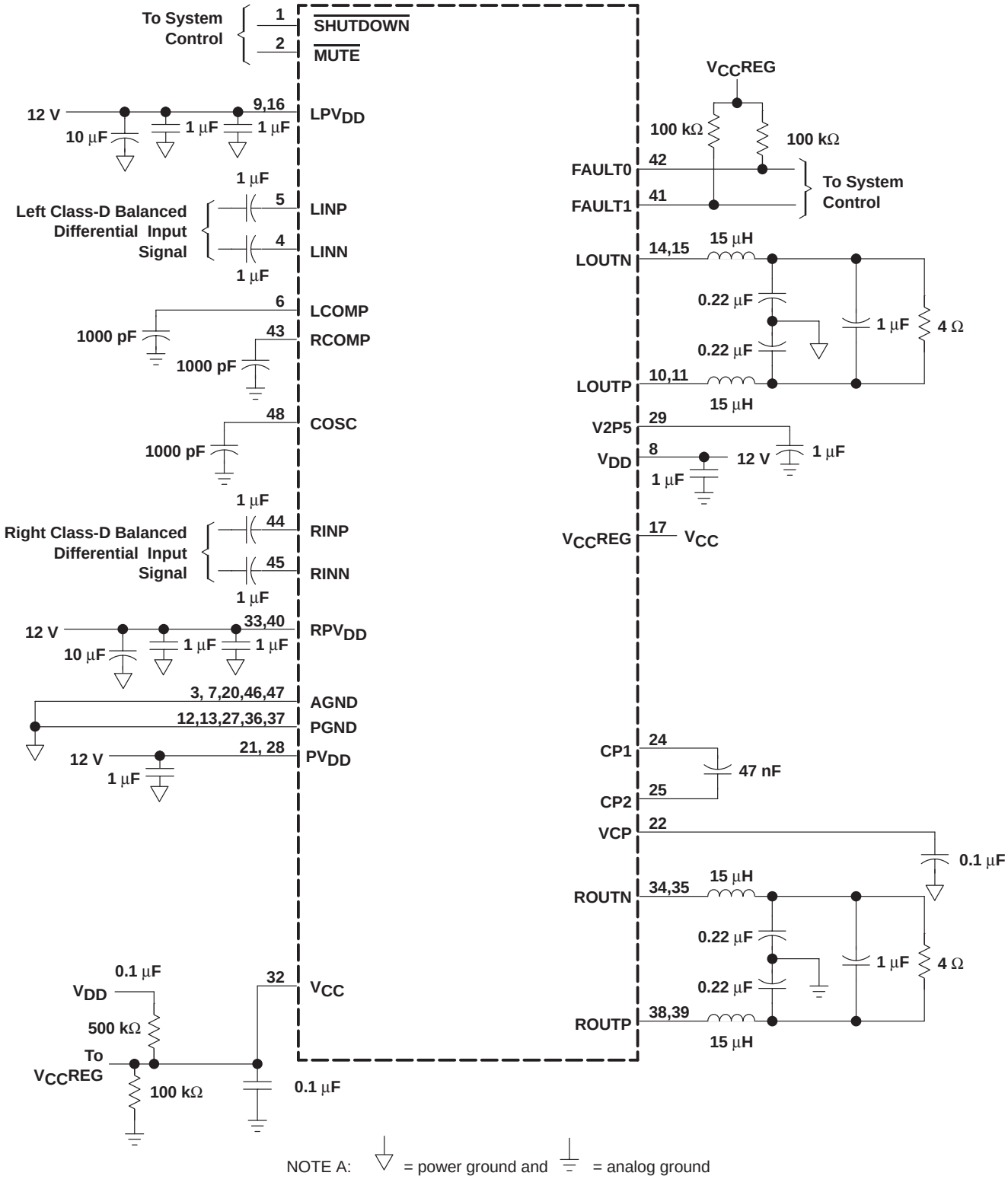


Figure 3. TPA032D02 Typical Configuration Application Circuit

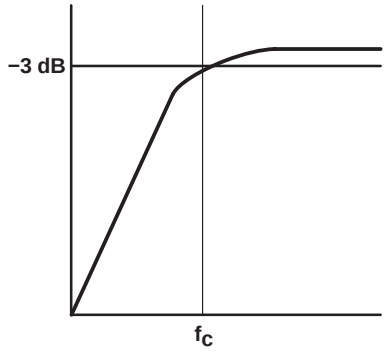
APPLICATION INFORMATION

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and Z_I, the TPA032D02's input resistance forms a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi Z_I C_I} \quad (8)$$

Z_I is nominally 10 kΩ



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi Z_I f_c} \quad (9)$$

In this example, C_I is 0.40 μF so one would likely choose a value in the range of 0.47 μF to 1 μF. A low-leakage tantalum or ceramic capacitor is the best choice for the input capacitors. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input, as the dc level there is held at 1.5 V, which is likely higher than the source dc level. Please note that it is important to confirm the capacitor polarity in the application.

differential input

The TPA032D02 has differential inputs to minimize distortion at the input to the IC. Since these inputs nominally sit at 1.5 V, dc-blocking capacitors are required on each of the four input terminals. If the signal source is single-ended, optimal performance is achieved by treating the signal ground as a signal. In other words, reference the signal ground at the signal source, and run a trace to the dc-blocking capacitor, which should be located physically close to the TPA032D02. If this is not feasible, it is still necessary to locally ground the unused input terminal through a dc-blocking capacitor.

power supply decoupling, C_S

The TPA032D02 is a high-performance Class-D CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF placed as close as possible to the device's various V_{DD} leads, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 μF or greater placed near the audio power amplifier is recommended.

The TPA032D02 has several different power supply terminals. This was done to isolate the noise resulting from high-current switching from the sensitive analog circuitry inside the IC.

APPLICATION INFORMATION

mute and shutdown modes

The TPA032D02 employs both a mute and a shutdown mode of operation designed to reduce supply current, I_{DD}, to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD} = 20 μA. Mute mode alone reduces I_{DD} to 10 mA.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

output filter components

The output inductors are key elements in the performance of the class-D audio amplifier system. It is important that these inductors have a high enough current rating and a relatively constant inductance over frequency and temperature. The current rating should be higher than the expected maximum current to avoid magnetically saturating the inductor. When saturation occurs, the inductor loses its functionality and looks like a short circuit to the PWM signal, which increases the harmonic distortion considerably.

A shielded inductor may be required if the class-D amplifier is placed in an EMI sensitive system; however, the switching frequency is low for EMI considerations and should not be an issue in most systems. The dc series resistance of the inductor should be low to minimize losses due to power dissipation in the inductor, which reduces the efficiency of the circuit.

Capacitors are important in attenuating the switching frequency and high frequency noise, and in supplying some of the current to the load. It is best to use capacitors with low equivalent-series-resistance (ESR). A low ESR means that less power is dissipated in the capacitor as it shunts the high-frequency signals. Placing these capacitors in parallel also parallels their ESR, effectively reducing the overall ESR value. The voltage rating is also important, and, as a rule of thumb, should be 2 to 3 times the maximum rms voltage expected to allow for high peak voltages and transient spikes. These output filter capacitors should be stable over temperature since large currents flow through them.

APPLICATION INFORMATION

efficiency of class-D vs linear operation

Amplifier efficiency is defined as the ratio of output power delivered to the load to power drawn from the supply. In the efficiency equation below, P_L is power across the load and P_{SUP} is the supply power.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

A high-efficiency amplifier has a number of advantages over one with lower efficiency. One of these advantages is a lower power requirement for a given output, which translates into less waste heat that must be removed from the device, smaller power supply required, and increased battery life.

Audio power amplifier systems have traditionally used linear amplifiers, which are well known for being inefficient. Class-D amplifiers were developed as a means to increase the efficiency of audio power amplifier systems.

A linear amplifier is designed to act as a variable resistor network between the power supply and the load. The transistors operate in their linear region and voltage that is dropped across the transistors (in their role as variable resistors) is lost as heat, particularly in the output transistors.

The output transistors of a class-D amplifier switch from full OFF to full ON (saturated) and then back again, spending very little time in the linear region in between. As a result, very little power is lost to heat because the transistors are not operated in their linear region. If the transistors have a low on-resistance, little voltage is dropped across them, further reducing losses. The ideal class-D amplifier is 100% efficient, which assumes that both the on-resistance ($r_{DS(on)}$) and the switching times of the output transistors are zero.

the ideal class-D amplifier

To illustrate how the output transistors of a class-D amplifier operate, a half-bridge application is examined first (see Figure 4).

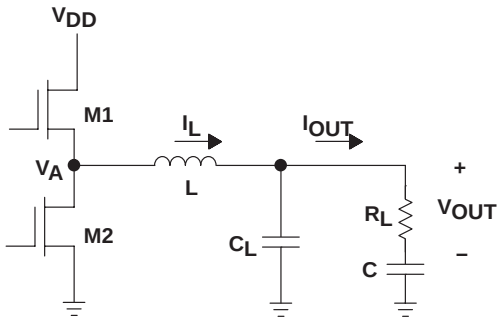


Figure 4. Half-Bridge Class-D Output Stage

Figures 5 and 6 show the currents and voltages of the half-bridge circuit. When transistor M1 is on and M2 is off, the inductor current is approximately equal to the supply current. When M2 switches on and M1 switches off, the supply current drops to zero, but the inductor keeps the inductor current from dropping. The additional inductor current is flowing through M2 from ground. This means that V_A (the voltage at the drain of M2, as shown in Figure 4) transitions between the supply voltage and slightly below ground. The inductor and capacitor form a low-pass filter, which makes the output current equal to the average of the inductor current. The low-pass filter averages V_A, which makes V_{OUT} equal to the supply voltage multiplied by the duty cycle.

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Control logic is used to adjust the output power, and both transistors are never on at the same time. If the output voltage is rising, M1 is on for a longer period of time than M2.

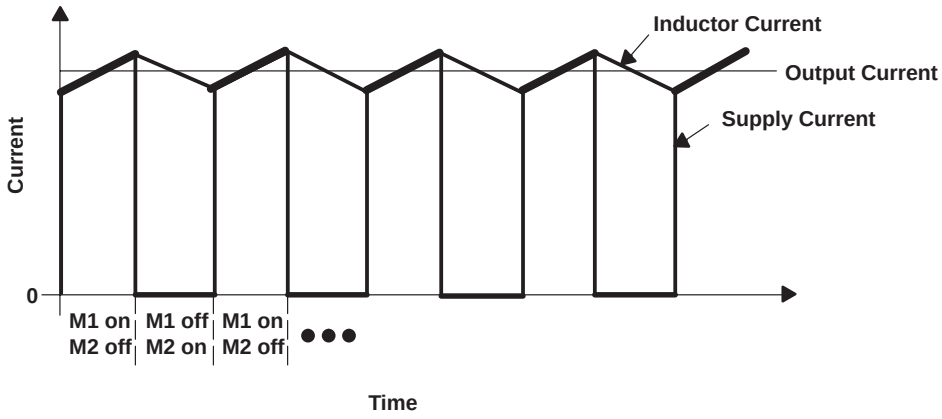


Figure 5. Class-D Currents

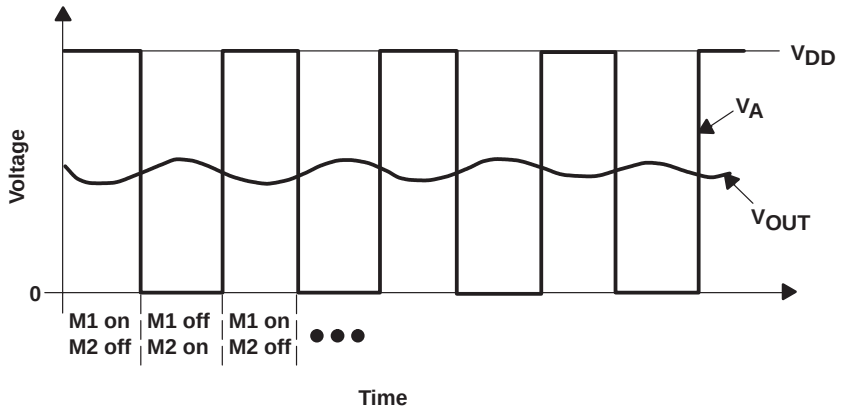


Figure 6. Class-D Voltages

APPLICATION INFORMATION

the ideal class-D amplifier (continued)

Given these plots, the efficiency of the class-D device can be calculated and compared to an ideal linear amplifier device. In the derivation below, a sine wave of peak voltage (V_P) is the output from an ideal class-D and linear amplifier and the efficiency is calculated.

CLASS-D	LINEAR
$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$	$V_{L(rms)} = \frac{V_P}{\sqrt{2}}$
$\text{Average}\left(I_{DD}\right) = \frac{I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$P_L = \frac{V_{L(rms)}^2}{R_L} = \frac{V_P^2}{2\,R_L}$
$P_L = V_L \times I_L$	$\text{Average}\left(I_{DD}\right) = \frac{2}{\pi} \times \frac{V_P}{R_L}$
$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right)$	$P_{SUP} = V_{DD} \times \text{Average}\left(I_{DD}\right) = \frac{V_{DD}\,V_P}{R_L} \times \frac{2}{\pi}$
$P_{SUP} = \frac{V_{DD} \times I_{L(rms)} \times V_{L(rms)}}{V_{DD}}$	$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$
$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$	$\text{Efficiency} = \eta = V_{DD} \times \frac{\frac{V_P^2}{2R_L}}{\frac{2}{\pi} \times \frac{V_P}{R_L}}$
$\text{Efficiency} = \eta = 1$	$\text{Efficiency} = \eta = \frac{\pi}{4} \times \frac{V_P}{V_{DD}}$

In the ideal efficiency equations, assume that $V_P = V_{DD}$, which is the maximum sine wave magnitude without clipping. Then, the highest efficiency that a linear amplifier can have without clipping is 78.5%. A class-D amplifier, however, can ideally have an efficiency of 100% at all power levels.

The derivation above applies to an H-bridge as well as a half-bridge. An H-bridge requires approximately twice the supply current but only requires half the supply voltage to achieve the same output power—factors that cancel in the efficiency calculation. The H-bridge circuit is shown in Figure 7.

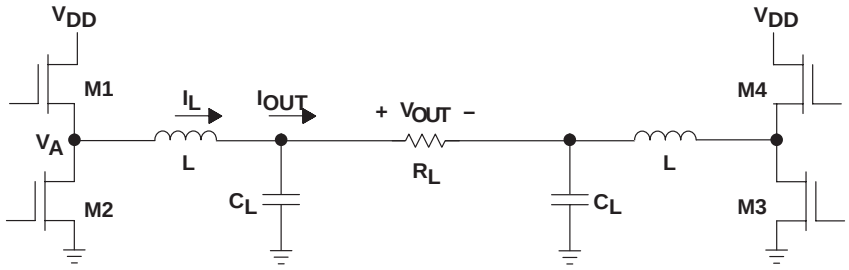


Figure 7. H-Bridge Class-D Output Stage

APPLICATION INFORMATION

losses in a real-world class-D amplifier

Losses make class-D amplifiers nonideal, and reduce the efficiency below 100%. These losses are due to the output transistors having a nonzero $r_{DS(on)}$, and rise and fall times that are greater than zero.

The loss due to a nonzero $r_{DS(on)}$ is called conduction loss, and is the power lost in the output transistors at nonswitching times, when the transistor is on (saturated). Any $r_{DS(on)}$ above 0 Ω causes conduction loss. Figure 8 shows an H-bridge output circuit simplified for conduction loss analysis and can be used to determine new efficiencies with conduction losses included.

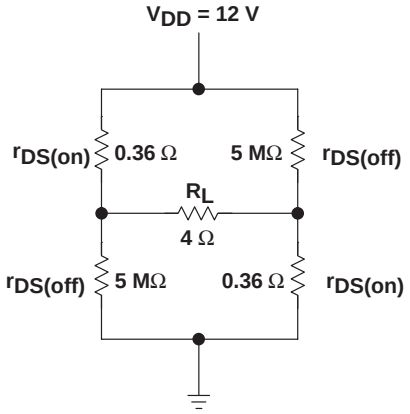


Figure 8. Output Transistor Simplification for Conduction Loss Calculation

The power supplied, P_{SUP}, is determined to be the power output to the load plus the power lost in the transistors, assuming that there are always two transistors on.

$$\text{Efficiency} = \eta = \frac{P_L}{P_{SUP}}$$

$$\text{Efficiency} = \eta = \frac{I^2 R_L}{I^2\, 2r_{DS(on)} + I^2 R_L}$$

$$\text{Efficiency} = \eta = \frac{R_L}{2r_{DS(on)} + R_L}$$

$$\text{Efficiency} = \eta = 95\% \left(\text{at all output levels } r_{DS(on)} = 0.1\ \Omega,\ R_L = 4\ \Omega\right)$$

$$\text{Efficiency} = \eta = 85\% \left(\text{at all output levels } r_{DS(on)} = 0.36\ \Omega,\ R_L = 4\ \Omega\right)$$

APPLICATION INFORMATION

losses in a real-world class-D amplifier (continued)

Losses due to rise and fall times are called switching losses. A diagram of the output, showing switching losses, is shown in Figure 9.

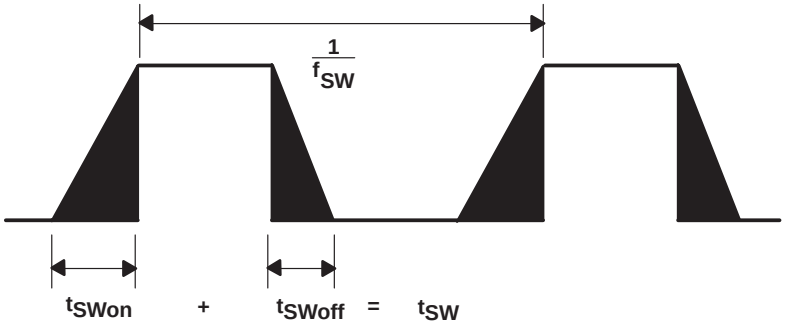


Figure 9. Output Switching Losses

Rise and fall times are greater than zero for several reasons. One is that the output transistors cannot switch instantaneously because (assuming a MOSFET) the channel from drain to source requires a specific period of time to form. Another is that transistor gate-source capacitance and parasitic resistance in traces form RC time constants that also increase rise and fall times.

Switching losses are constant at all output power levels, which means that switching losses can be ignored at high power levels in most cases. At low power levels, however, switching losses must be taken into account when calculating efficiency. Switching losses are dominated by conduction losses at the high output powers, but should be considered at low powers. The switching losses are automatically taken into account if you consider the quiescent current with the output filter and load.

class-D effect on power supply

Efficiency calculations are an important factor for proper power supply design in amplifier systems. Table 2 shows Class-D efficiency at a range of output power levels (per channel) with a 1-kHz sine wave input. The maximum power supply draw from a stereo 10-W per channel audio system with 4-Ω loads and a 12-V supply is almost 26 W. A similar linear amplifier such as the TPA032D02 has a maximum draw of greater than 50 W under the same circumstances.

Table 2. Efficiency vs Output Power in 12-V 4-Ω H-Bridge Systems

Output Power (W)	Efficiency (%)	Peak Voltage (V)	Internal Dissipation (W)
0.5	41.7	2	0.7
2	66.7	4	1.0
5	75.1	6.32	1.66
8	78	8	2.26
10	77.9	8.94†	2.84

† High peak voltages cause the THD to increase

APPLICATION INFORMATION

class-D effect on power supply (continued)

There is a minor power supply savings with a class-D amplifier versus a linear amplifier when amplifying sine waves. The difference is much larger when the amplifier is used strictly for music. This is because music has much lower RMS output power levels, given the same peak output power (see Figure 10); and although linear devices are relatively efficient at high RMS output levels, they are very inefficient at mid-to-low RMS power levels. The standard method of comparing the peak power to RMS power for a given signal is crest factor, whose equation is shown below. The lower RMS power for a set peak power results in a higher crest factor

$$\text{Crest Factor} = 10 \log \frac{P_{PK}}{P_{rms}}$$

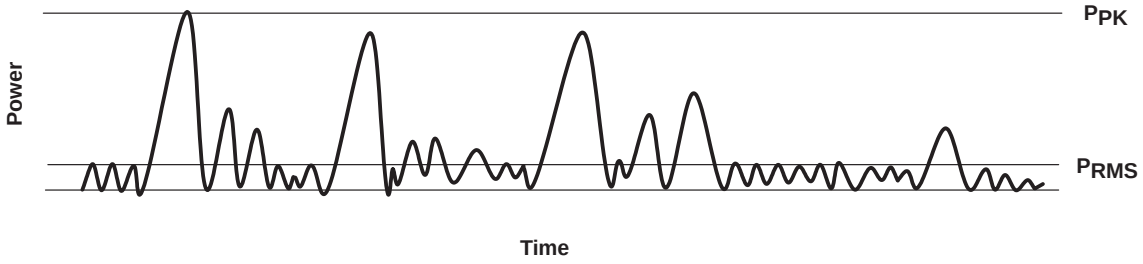


Figure 10. Audio Signal Showing Peak and RMS Power

APPLICATION INFORMATION

class-D EVM power supply decoupling data

The decoupling capacitance required will depend upon the application. Pads and through-holes have been provided on the EVM for the addition of bulk capacitance (see the schematic). A plot showing the impact of various levels of bulk capacitance on the voltage ripple on the power supply line is shown in Figure 11. This ripple is maximum at higher frequency. The figure shows worst-case voltage ripple for a 20-kHz, 10-W output into a 4-Ω load. In all cases, two 10-μF and one 1-μF ceramic chip capacitors were decoupling the power supply signal from the EVM. The 1-μF unit was placed immediately adjacent to the IC power pins, and the 10-μF units were placed adjacent to each other a little farther out.

The upper trace shows the ripple when only these capacitors are used. The middle trace shows the impact of an additional 330-μF aluminum electrolytic capacitor rated at 25 V, 90 mΩ, and for 755 mA at 100 kHz. In the bottom trace, the 330-μF capacitor was replaced by a 390-μF aluminum electrolytic capacitor rated at 35 V, 65 mΩ, and for 1.2 A of 100 kHz ripple current.

The results indicate that for sensitive circuits where minimum voltage ripple is required, a larger bulk capacitance with low ESR should be used. For systems that are contained and EMI is controlled, less capacitance may be used. The difference in the level of distortion in the output signal was very small between each level of decoupling, with the 20-μF bulk capacitance providing the least distortion. This is attributed to the low ESR of the capacitor, which is only a few milliohms at the switching frequency of 250 kHz. The distortion is made lower still by the parallel combination. Distortion of the output signal when only one 10-μF capacitor is used is the same as for 20 μF. The difference is more noticeable on the power supply line, though the distortion is increased only slightly more than with the 20-μF capacitor.

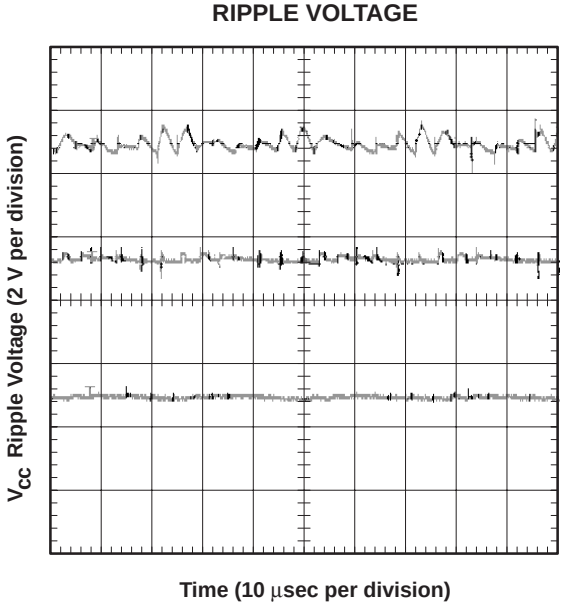


Figure 11. Power Supply Decoupling

APPLICATION INFORMATION

crest factor and thermal considerations

A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA032D02 data sheet, one can see that when the TPA032D02 is operating from a 12-V supply into a 4-Ω speaker that 20-W peaks are available. Converting watts to dB:

$$P_{dB} = 10\,\text{Log}\left(\frac{P_W}{P_{ref}}\right) = 10\text{Log}\left(\frac{20}{1}\right) = 6\text{ dB} \tag{17}$$

Subtracting the crest factor restriction to obtain the average listening level without distortion yields:

6.0 dB − 18 dB = − 12 dB (15 dB crest factor)
6.0 dB − 15 dB = − 9 dB (15 dB crest factor)
6.0 dB − 12 dB = − 6 dB (12 dB crest factor)
6.0 dB − 9 dB = − 3 dB (9 dB crest factor)
6.0 dB − 6 dB = − 0 dB (6 dB crest factor)
6.0 dB − 3 dB = 3 dB (3 dB crest factor)

Converting dB back into watts:

$$P_W = 10^{PdB/10} \times P_{ref} \tag{18}$$

= 315 mW (18 dB crest factor)
= 630 mW (15 dB crest factor)
= 1.25 W (12 dB crest factor)
= 2.5 W (9 dB crest factor)
= 5 W (6 dB crest factor)
= 10 W (3 dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 10 W of continuous power output with a 3 dB crest factor, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 12-V, 4-Ω system, the internal dissipation in the TPA032D02 and maximum ambient temperatures are shown in Table 3.

APPLICATION INFORMATION

crest factor and thermal considerations (continued)

Table 3. TPA032D02 Power Rating, 12-V, 4-Ω, Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE
20	10 W (3 dB)	2.84	23°C
20	5 W (6 dB)	1.66	75°C
20	2.5 W (9 dB)	1.12	100°C
20	1.25 W (12 dB)	0.87	111°C
20	630 mW (15 dB)	0.7	118°C
20	315 mW (18 dB)	0.6	123°C

The maximum ambient temperature depends on the heatsinking ability of the PCB system. Using the 0 CFM data from the dissipation rating table, the derating factor for the DCA package with 6.9 in^2 of copper area on a multilayer PCB is 44.8 mW/°C. Converting this to Θ_{JA}:

$$\Theta_{JA} = \frac{1}{\text{Derating}} \tag{19}$$

$$= \frac{1}{0.0448}$$

$$= 22.3°C/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel so the dissipated heat needs to be doubled for two channel operation. Given Θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated with the following equation. The maximum recommended junction temperature for the TPA032D02 is 150 °C. The internal dissipation figures are taken from the Efficiency vs Output Power graphs.

$$T_A\,\text{Max} = T_J\,\text{Max} - \Theta_{JA}\,P_D \tag{20}$$

$$= 150 - 22.3(0.7 \times 2) = 118°C \text{ (15 dB crest factor)}$$

$$= 150 - 22.3(2.84 \times 2) = 23°C \text{ (3dB crest factor)}$$

NOTE:
Internal dissipation of 1.4 W is estimated for a 10-W system with a 15 dB crest factor per channel.

The TPA032D02 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 3 was calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

THERMAL INFORMATION

The thermally enhanced DCA package is based on the 56-pin TSSOP, but includes a thermal pad (see Figure 12) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface-mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

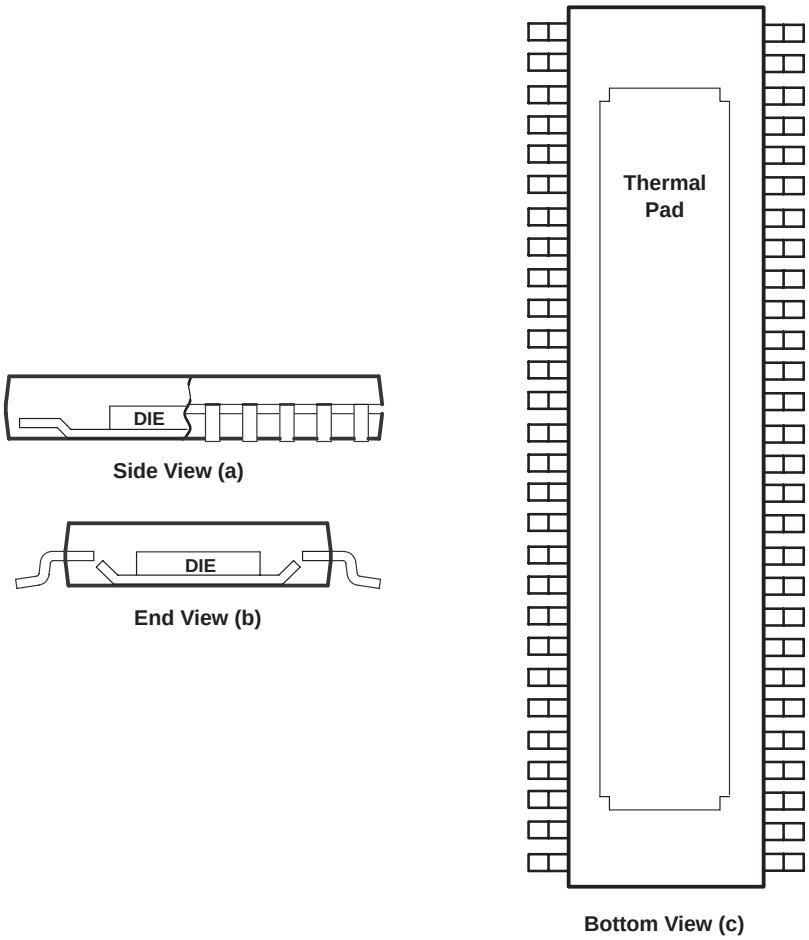


Figure 12. Views of Thermally Enhanced DCA Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA032D02DCA	OBSOLETE	HTSSOP	DCA	48		TBD	Call TI	Call TI	-40 to 125	TPA032D02	
TPA032D02DCAG4	OBSOLETE	HTSSOP	DCA	48		TBD	Call TI	Call TI	-40 to 125		
TPA032D02DCAR	OBSOLETE	HTSSOP	DCA	48		TBD	Call TI	Call TI	-40 to 125	TPA032D02	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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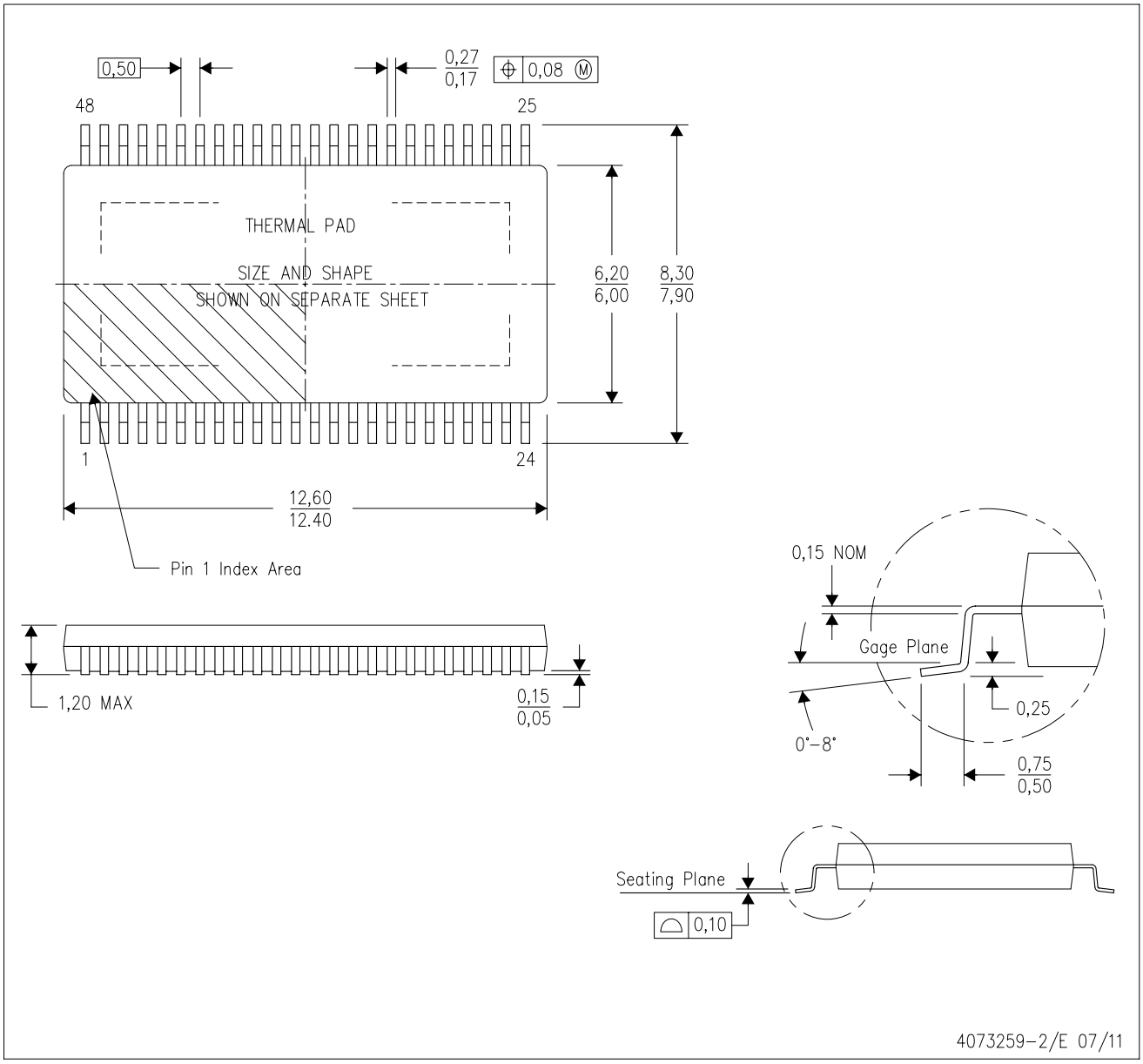
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

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