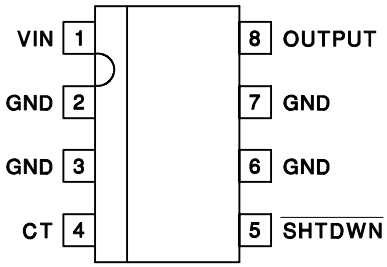
UCC39161
LOW CURRENT HOT SWAP POWER MANAGER

SLUS410C – NOVEMBER 1999 – REVISED FEBRUARY 2000

- **Integrated Circuit Breaker Function**
- **Integrated 0.2-Ω Power FET**
- **1μA I_{CC} When Disabled**
- **Programmable On Time**
- **Accurate 0.8-A (MAX) Current**
- **Fixed 3% Duty Cycle**
- **Unidirectional Switch**
- **Thermal Shutdown**

SOIC 8-PIN
DP PACKAGE
(TOP VIEW)



description

The UCC39161 low-current hot-swap power manager provides complete power management, hot-swap capability, and circuit-breaker functions with minimal external components. For most applications, the only external component required to operate the device, other then supply bypassing, is a timing capacitor that sets the fault time.

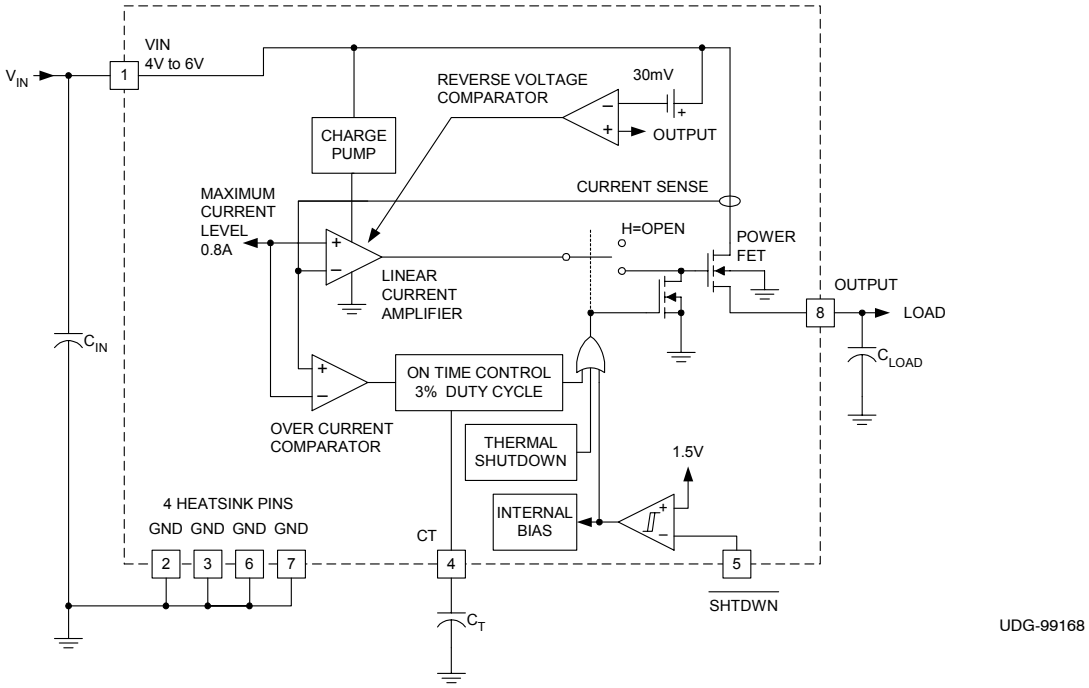
The maximum current level is internally programmed for 0.8 A. While the output current is below 0.8 A, the internal power MOSFET is switched on at a nominal 220 mΩ. When the output current exceeds 0.8 A, the MOSFET transitions from a switch to a constant current source and the fault timer starts charging CT. Once the fault time is reached, the current shuts off for a time, which equates to a 3% duty cycle.

The UCC39161 also provides unidirectional current flow, emulating a diode in series with the power MOSFET.

The UCC39161 can be put into sleep mode by grounding the $\overline{\text{SHTDWN}}$ pin. In sleep mode, the UCC39161 draws under 5 μA of supply current.

Other features include thermal shutdown and a low thermal-resistance small-outline power package.

block diagram



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absolute maximum ratings over operating free-air temperature (unless otherwise noted)†‡

Input voltage (VIN) . . . . . 6 V
Output current, dc . . . . . Self Limiting
Output current, pulse (less than 100 ns) . . . . . 20 A
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10 sec) . . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

electrical characteristics at T_J = 0°C to 70°C, VIN = 5 V, $\overline{\text{SHTDWN}}$ = 2.4 V, $T_A = T_J$ (unless otherwise noted) (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
I_{CC} supply current			1.00	2.00	mA
I_{CC} supply current (sleep mode)	$\overline{\text{SHTDWN}}$ = 0.2 V		0.50	5	μA
Output Section					
Voltage drop	I_{OUT} = 0.5 A		0.10	0.16	V
Max current		–1.0	–0.8	–0.6	A
Reverse leakage	VIN = 4.5 V, V_{OUT} = 5 V		6	20	μA
	VIN = 0 V, V_{OUT} = 5 V		0.50	9	μA
Soft start time	Initial Startup		50		μs
Short circuit response			100		ns
Fault Section					
CT charge current	V_{CT} = 1.0 V	–45	–36.0	–27	μA
CT discharge current	V_{CT} = 1.0 V	0.90	1.0	1.50	μA
Output duty cycle	V_O = 0 V	2.00	3.00	6.00	%
CT charge threshold		0.4	0.5	0.6	V
CT discharge threshold		1.2	1.4	1.8	V
Thermal shutdown			170		°C
Thermal hysteresis			10		°C
Shutdown Section					
Shutdown threshold			1.5	3.0	V
Shutdown hysteresis			150	300	mV
Shutdown bias current	$\overline{\text{SHTDWN}}$ = 1.0 V		100	500	nA

NOTE: All voltages are with respect to ground.

pin description

CT: A capacitor is applied between this pin and ground to set the maximum fault time. The maximum fault time must be more than the time to charge external capacitance. The maximum fault time is defined as:

$$T_{FAULT} = 28 \times 10^3 \times CT$$

Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 1 \times 10^6 \times CT$$

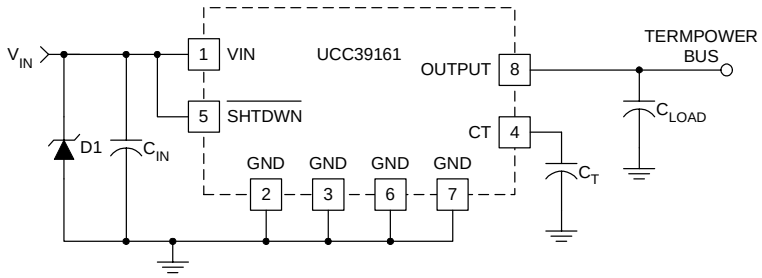
this results in a 3% duty cycle.

$\overline{\text{SHTDWN}}$: The IC enters a low-power sleep mode when this pin is low and exits the sleep mode when this pin is high.

VIN: Input voltage to the circuit breaker, ranging from 4 V to 6 V.

VOUT: Output voltage of the circuit breaker. When switched, the output voltage is approximately:

$$V_{OUT} = VIN - 220\ m\Omega \times I_{OUT}$$



UDG-99167

Figure 1. Typical Application

APPLICATION INFORMATION

protecting the ucc39161 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC39161. *It is important to limit the peak of this spike to less than 6 V to prevent damage to the UCC39161.* This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive (+) and negative (–) leads of the power supply feeding V_{IN}, locate the power supply close to the UCC39161 or use a PCB ground plane).
- Decoupling V_{IN} with a capacitor, C_{IN} (refer to Figure 1), located close to the VIN pin. This capacitor is typically less than 1 μF to limit the inrush current.
- Clamping the voltage at V_{IN} below 6 V with a zener diode, D1 (refer to Figure 1), located close to the VIN pin.

APPLICATION INFORMATION

safety recommendations

Although the UCC39161 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC39161 is intended for use in safety critical applications where UL™ or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC39161 prevents the fuse from blowing virtually all fault conditions, increasing system reliability and reducing maintainence cost, in addition to providing the hot-swap benefits of the device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCC39161DP	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	Samples Not Available
UCC39161DPG4	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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