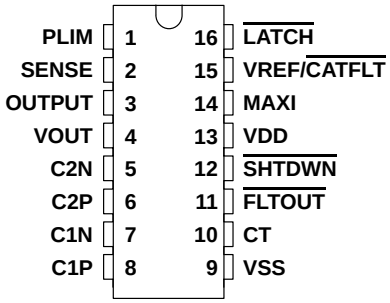
UCC2917, UCC3917
POSITIVE FLOATING HOT-SWAP POWER MANAGER

SLUS203B – FEBRUARY 2000 – REVISED AUGUST 2000

- **Manages Hot-Swap of 15 V and Above**
- **Precision Fault Threshold**
- **Programmable Average Power Limiting**
- **Programmable Linear Current Control**
- **Programmable Overcurrent Limit**
- **Programmable Fault Time**
- **Internal Charge Pump to Control External NMOS Device**
- **Fault Output and Catastrophic Fault Indication**
- **Fault Mode Programmable to Latch or Retry**
- **Shutdown Control**
- **Undervoltage Lockout**

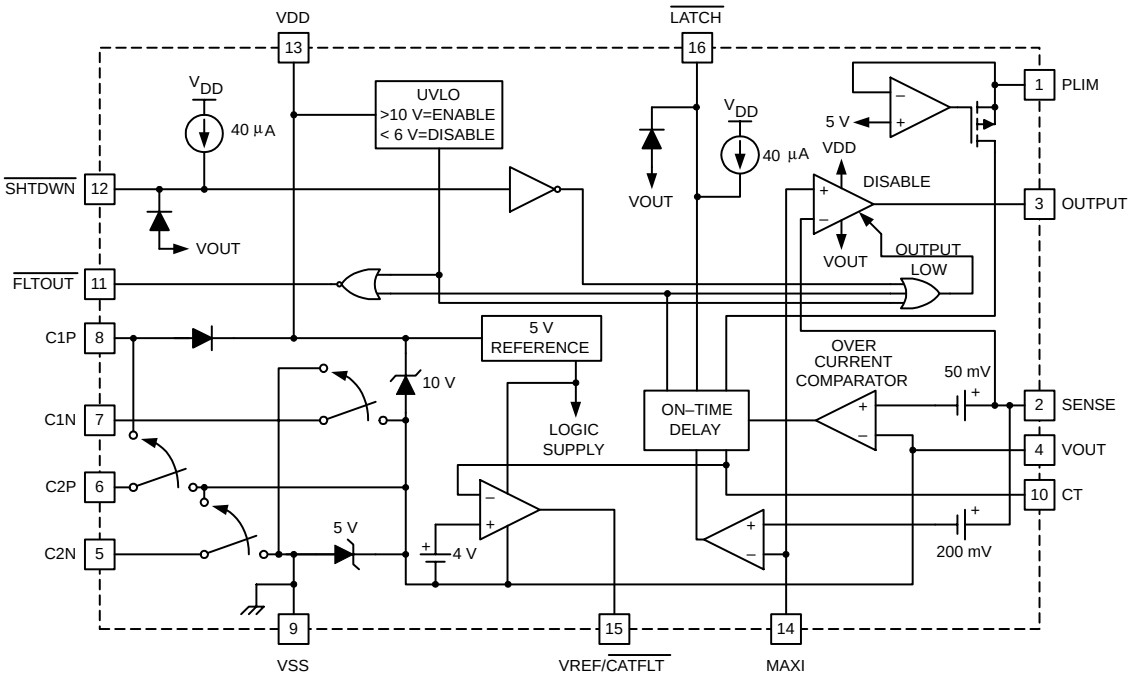
D, J, AND N PACKAGE
(TOP VIEW)



description

The UCCx917 family of positive-floating hot-swap managers provides complete power management, hot-swap, and fault handling capability. The voltage limitation of the application is only restricted by the external component voltage limitations. The IC provides its own supply voltage via a charge pump referenced to VOUT. The onboard 10-V shunt regulator protects the IC from excess voltage. The IC also has catastrophic fault indication to alert the user that the ability to shut off the output NMOS has been bypassed. All control and housekeeping functions are integrated and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft-start time, and average NMOS power limiting.

block diagram



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description (continued)

The fault level across the current-sense amplifier is fixed at 50 mV to minimize total drop out. Once 50 mV is exceeded across the current-sense resistor, the fault timer starts. The maximum allowable sourcing current is programmed with a voltage divider from the VREF/$\overline{\text{CATFLT}}$ pin to generate a fixed voltage on the MAXI pin. The current level at which the output appears as a current source is equal to V_{MAXI} divided by the current-sense resistor. If desired, a controlled current startup can be programmed with a capacitor on MAXI.

When the output current is below the fault level, the output device is switched on with full gate drive. When the output current exceeds the fault level, but is less than maximum allowable sourcing level programmed by MAXI, the output remains switched on, and the fault timer starts charging the timing capacitor C_T. Once C_T charges to 2.5 V, the output device is turned off and attempts either a retry sometime later or waits for the state on the $\overline{\text{LATCH}}$ pin to change if in latch mode. When the output current reaches the maximum sourcing current level, the output device appears as a current source.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply current . . . . . 20 mA
$\overline{\text{SHTDWN}}$ current . . . . . –500 μA
$\overline{\text{LATCH}}$ current . . . . . –500 μA
VREF current . . . . . –500 μA
PLIM current . . . . . 10 mA
MAXI input voltage . . . . . V_{DD} + 0.3 V
Junction temperature, T_J . . . . . –55°C to 150°C
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Lead temperature (Soldering, 10 sec.) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Interface Products Data Book (TI Literature Number SLUD002) for thermal limitations and considerations of package.

ORDERING INFORMATION

T_J	PACKAGED DEVICES		
	DIP (J)	DIP (N)	SOIC (D)
–40°C to 85°C	UCC2917J	UCC2917N	UCC2917D
0°C to 70°C	UCC3917J	UCC3917N	UCC3917D

electrical characteristics, T_A = 0°C to 70°C for the UCC3917, –40°C to 85°C for the UCC2917, C_T = 4.7 nF, $T_A = T_J$, all voltages are with respect to VOUT, current is positive into and negative out of the specified terminal, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
I_{DD}, supply current	From VOUT, See Note 1	4.0	5	11	mA
UVLO turn on threshold		7.9	8.8	9.7	V
UVLO off voltage		5.5	6.5	7.5	V
VSS regulator voltage		–6	–5	–4	V

NOTE 1: Set by user with R_{SS}.

electrical characteristics, T_A = 0°C to 70°C for the UCC3917, –40°C to 85°C for the UCC2917, C_T = 4.7 nF, $T_A = T_J$, all voltages are with respect to VOUT, current is positive into and negative out of the specified terminal, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fault Timing Section					
Overcurrent threshold	T_A = 25°C	47.5	50	53	mV
	Over operating temperature	46	50	54	mV
Overcurrent input bias			50	500	nA
CT charge current	V_{CT} = 1 V	–78	–50	–28	µA
CT catastrophic fault threshold		3.4		4.5	V
Fault Timing Section (continued)					
CT fault threshold		2.25	2.5	2.75	V
CT reset threshold		0.32	0.5	0.62	V
Output duty cycle	Fault condition	1.7%	2.7%	3.7%	
Output Section					
Output high voltage	I_{OUT} = 0	6	8	10	V
	I_{OUT} = –100 µA	5	7	9	V
Output low voltage	I_{OUT} = 500 µA		0.03	0.50	V
	I_{OUT} = 1 mA		0.6	0.9	V
Linear Current Section					
Sense control voltage	MAXI = 100 mV	85	100	115	mV
	MAXI = 400 mV	370	400	430	mV
Input bias	MAXI = 200 mV		50	500	nA
$\overline{\text{SHUTDOWN}}$ Section					
Shutdown threshold		2.0	2.4	2.8	V
Input current	$\overline{\text{SHTDWN}}$ = 0 V	24	40	60	µA
Shutdown delay			100	500	ns
$\overline{\text{LATCH}}$ Section					
Latch threshold		1.7	2	2.3	V
Input current	$\overline{\text{LATCH}}$ = 0 V	24	40	60	µA
$\overline{\text{FLTOUT}}$ Section					
Fault output high	V_{CT} = 0 V, I_{SOURCE} = 0 µA	6	8	10	V
Fault output low	V_{CT} = 5 V, I_{SINK} = 200 µA		0.01	0.05	V
Power Limiting Section					
V_{SENSE} regulator voltage	I_{PLIMIT} = 64 µA	4.5	5	5.5	V
Duty cycle control	I_{PLIMIT} = 64 µA	0.6%	1.2%	1.7%	
	I_{PLIMIT} = 1 mA	0.045%	0.1%	0.2%	
VREF/$\overline{\text{CATFLT}}$ Section					
V_{REF} regulator voltage		4.5	5	5.5	V
Fault output low	$I_{VREF/\overline{CATFLT}}$ = 5 mA		0.22	0.50	V
Output sink current	V_{CT} = 5 V, $V_{VREF/\overline{CATFLT}}$ = 5 V	15	40	70	mA
Overload comparator threshold	Relative to MAXI	110	200	290	mV

pin assignments

C1N: Negative side of the upper charge-pump capacitor.

C1P: Positive side of the upper charge-pump capacitor.

C2N: Negative side of the lower charge-pump capacitor.

C2P: Positive side of lower charge-pump capacitor.

CT: A capacitor is connected to this pin to set the fault time. The fault time must be more than the time to charge the external load capacitance (see application information).

$\overline{\text{FLTOUT}}$: This pin provides fault output indication. Interface to this pin is usually performed through level-shift transistors. Under a non-fault condition, $\overline{\text{FLTOUT}}$ is pulled to a high state. When a fault is detected by the fault timer or the undervoltage lockout, this pin is driven to a low state, indicating the output NMOS is in the off state.

$\overline{\text{LATCH}}$: Pulling this pin low causes a fault to latch until this pin is brought high or a power-on reset is attempted. However, pulling this pin high before the reset time is reached does not clear the fault until the reset time is reached. Keeping $\overline{\text{LATCH}}$ high results in normal operation of the fault timer. Users should note there will be an RC delay dependent upon the external capacitor at this pin.

MAXI: This pin programs the maximum-allowable sourcing current. Since VREF/$\overline{\text{CATFLT}}$ is a regulated voltage, a voltage divider can be derived to generate the program level for MAXI. The current level at which the output appears as a current source is equal to the voltage on MAXI divided by the current-sense resistor. If desired, a controlled current start-up can be programmed with a capacitor on MAXI (to VOUT), and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUTPUT: Gate drive to the NMOS pass element.

PLIM: This feature ensures that the average external NMOS power dissipation is controlled. A resistor is connected from this pin to the drain of the external NMOS pass element. When the voltage across the NMOS exceeds 5 V, current flows into PLIM, which adds to the fault timer charge current, reducing the duty cycle from the 3% level.

SENSE: Input voltage from the current-sense resistor. When there is greater than 50 mV across this pin with respect to VOUT, a fault is sensed, and C_T starts to charge.

$\overline{\text{SHTDWN}}$: This pin provides shutdown control. Interface to this pin is usually performed through level-shift transistors. When shutdown is driven low, the output disables the NMOS pass device.

VDD: Power to the IC is supplied by an external current-limiting resistor on initial power up or if the load is shorted. As the load voltages rises (VOUT), a small amount of power is drawn from VOUT by an internal charge pump. The charge pump's input voltage is regulated by an on-chip 5-V zener. Power to VDD is supplied by the charge pump under normal operation (i.e., external FET is on).

VOUT: Ground reference for the IC.

VREF/$\overline{\text{CATFLT}}$: This pin primarily provides an output reference for the programming of MAXI. Secondarily, it provides catastrophic fault indication. In a catastrophic fault, when the IC unsuccessfully attempts to shutdown the NMOS pass device, this pin pulls to a low state when C_T charges above the catastrophic fault threshold. A possible application for this pin is to trigger the shutdown of an auxiliary FET in series with the main FET for redundancy.

VSS: Negative reference out of the chip. This pin is normally current fed via a resistor to load ground.

APPLICATION INFORMATION

fault timing

Figure 1 shows the detailed circuitry for the fault timing function of the UCC3917. For simplicity, first consider a typical fault mode where the overload comparator and the current source I3 do not come into play. A typical fault occurs once the voltage across the current-sense resistor, R_S, exceeds 50 mV. This causes the overcurrent comparator to trip and the timing capacitor to charge with current source I1 plus the current from the power limiting amplifier, or PLIM amplifier. The PLIM amplifier is designed to only source current into the CT pin once the voltage across the output FET exceeds 5 V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{\left(V_{IN} - VOUT\right) - 5\ V}{R_{PL}}$$

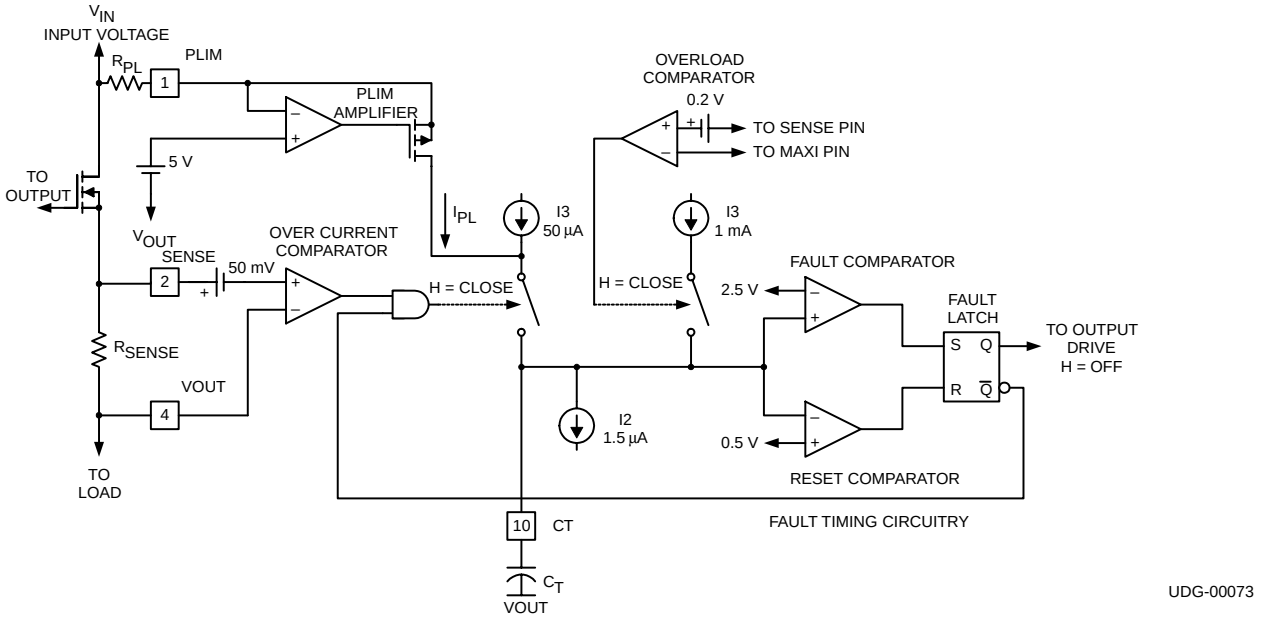

Figure 1. Fault Timing Circuitry for the UCC3917, Including Power Limit and Overload

Note that under normal fault conditions where the output current is just above the fault level, VOUT ≅ V_{IN}, I_{PL} = 0, and the C_T charging current is just I1.

During a fault, C_T charges at a rate determined by the internal charging current and the external timing capacitor, C_T. Once C_T charges to 2.5 V, the fault comparator switches and sets the fault latch. Setting the fault latch causes both the output to switch off and the charging switch to open. C_T must now discharge with current source I2 until 0.5 V is reached. Once the voltage at C_T reaches 0.5 V, the fault latch resets (assuming $\overline{\text{LATCH}}$ is high, otherwise the fault latch does not reset until the $\overline{\text{LATCH}}$ pin is brought high or a power-on reset occurs). This re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the overcurrent comparator closes the charging switch causing the cycle to repeat. Under a constant fault the duty cycle is given by:

$$\text{Duty Cycle} = \frac{I2}{I_{PL} + I1} \cong \frac{1.5\ \mu A}{I_{PL} + 50\ \mu A}$$

where I_{PL} is 0 µA under normal operations (see Figure 2).

APPLICATION INFORMATION

fault timing (continued)

However, under large transients, average power dissipation can be limited using the PLIM pin. A proof follows, average dissipation in the pass element is given by:

$$P_{FET(avg)} = \left(V_{IN} - VOUT\right) \times I_{MAX} \times \text{Duty Cycle} = \left(V_{IN} - VOUT\right) \times I_{MAX} \times \frac{1.5\ \mu A}{I_{PL} + 50\ \mu A}$$

Where (V_{IN} – VOUT) >>5 V,

$$I_{PL} \cong \frac{V_{IN} - VOUT}{R_{PL}}$$

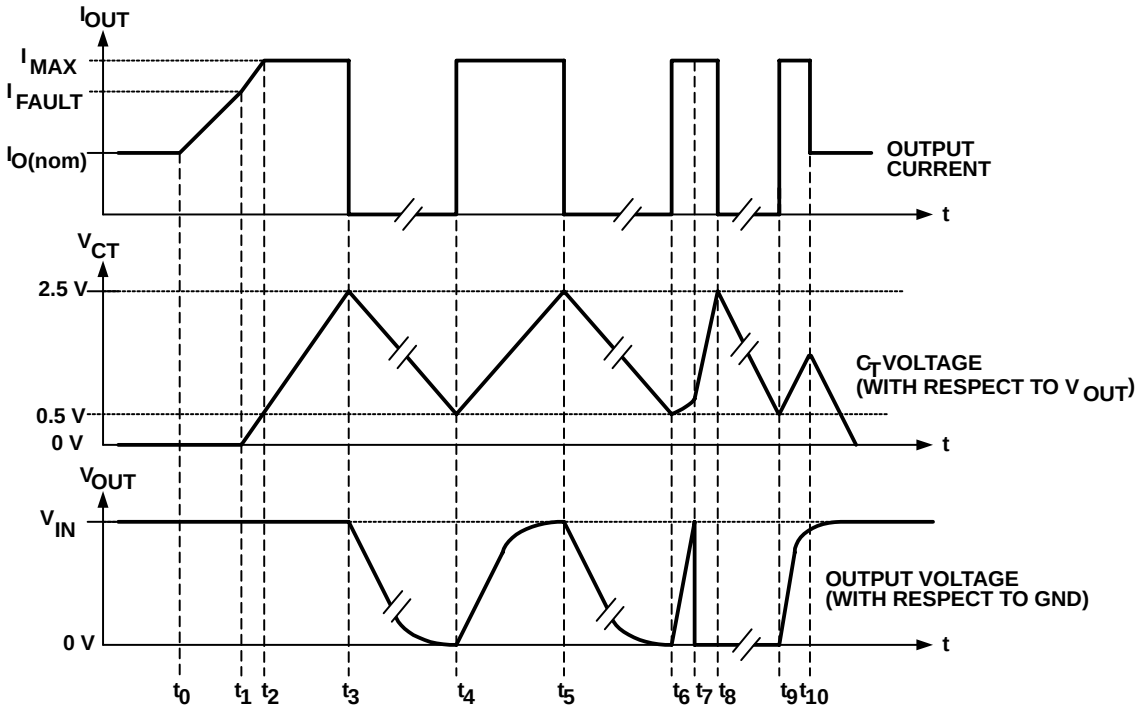

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Figure 2. Nominal Timing Diagram

APPLICATION INFORMATION

fault timing (continued)

t0: Safe condition - output current is nominal, output voltage is at the positive rail, V_{IN}.

t1: Fault control reached - output current rises above the programmed fault value, C_T begins to charge with $\cong$ 50 μA.

t2: Maximum current reached - output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: Fault occurs - C_T has charged to 2.5 V, fault output goes low, the FET turns off allowing no output current to flow, VOUT discharges to ground.

t4: Retry - C_T has discharged to 0.5 V, but fault current is still exceeded, C_T begins charging again, FET is on, VOUT rises to V_{IN}.

t5 = t3: Illustrates 3% duty cycle.

t6 = t4:

t7: Output short circuit - if VOUT is short circuited to ground, C_T charges at a higher rate depending upon the values for V_{IN} and R_{PL}.

t8: Fault occurs - output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9: Output short circuit released, still in fault mode.

t10 = t0: Fault released, safe condition - return to normal operation of the circuit breaker.

Note that t6 – t5 $\cong$ 36 $\times$ (t5 – t4).

and where I_{PL} >> 50 μA, the duty cycle can be approximated as:

$$\frac{1.5\ \mu A \times R_{PL}}{V_{IN} - VOUT}$$

Therefore the average power dissipation in the MOSFET can be approximated by:

$$P_{FET(avg)} = \left(V_{IN} - VOUT\right) \times I_{MAX} \times \frac{1.5\ \mu A \times R_{PL}}{V_{IN} - VOUT} = I_{MAX} \times 1.5\ \mu A \times R_{PL}$$

Notice that since (V_{IN} – VOUT) cancels, average power dissipation is limited in the NMOS pass element (see Figure 3). Also, a value for R_{PL} can be roughly determined from this approximation.

$$R_{PL} = \frac{P_{FET(avg)}}{I_{MAX} \times 1.5\ \mu A}$$

APPLICATION INFORMATION

fault timing (continued)

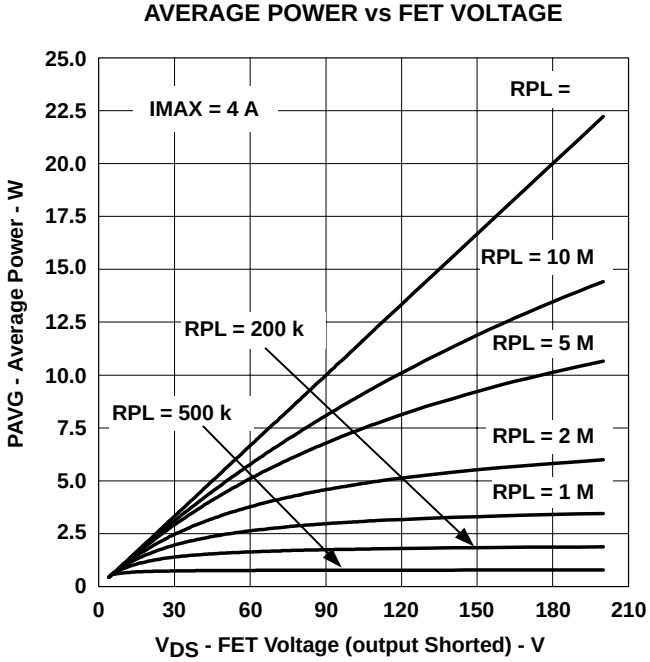


Figure 3.

overload comparator

The overload comparator provides protection against a shorted load during normal operation when the external N-channel FET is fully enhanced. Once the FET is fully enhanced the linear current amplifier essentially saturates and the system is in effect operating open loop. Once the FET is fully enhanced the linear current amplifier requires a finite amount of time to respond to a shorted output possibly destroying the external FET. The overload comparator is provided to quickly shutdown the external MOSFET in the case of a shorted output (if the FET is fully enhanced). During an output short, C_T is charged by I3 at ≈ 1 mA. The current threshold for the overload comparator is a function of I_{MAX} and a fixed offset and is defined as:

$$I_{OVERLOAD} = I_{MAX} + 200\ mV/R_S$$

Once the overcurrent comparator trips, the UCC3917 enters a programmed fault mode (hiccup or latched). It should be noted that on subsequent retries during hiccup mode or if a short should occur when the UCC3917 is actively limiting the current, the output current will not exceed I_{MAX}. In the event that the external FET does not respond during a fault the UCC3917 will set the VREF/$\overline{\text{CATFLT}}$ pin low to indicate a catastrophic failure.

APPLICATION INFORMATION

selecting the minimum timing capacitance

To ensure that the IC starts up correctly the designer must ensure that the fault time programmed by C_T exceeds the startup time of the load. The startup time (t_{START}) is a function of several components; load resistance and load capacitance, soft-start components R1, R2 and C_{SS}, the power limit current contribution determined by R_{PL}, and C_{IN}.

For a parallel capacitor-constant current load:

$$t_{START} = \frac{C_{LOAD} \times VIN}{I_{MAX} - I_{LOAD}} \tag{1}$$

For a parallel R-C load:

$$t_{START} = R_{LOAD} \times C_{LOAD} \times \ell n\left[1 - \frac{V_{IN}}{I_{MAX} \times R_{LOAD}}\right] \tag{2}$$

If the power limit function is not be used then $C_{T(min)}$ can be easily found:

$$C_{T(min)} = \frac{I_{CH} \times t_{START}}{dV_{CT}} \tag{3}$$

where dV_{CT} is the hysteresis on the fault detection circuitry. During operation in the latched fault mode configuration dV_{CT} = 2.5 V. When the UCC3917 is configured for the hiccup or retry mode of fault operation dV_{CT} = 2.0 V.

If the power limit function is used, the C_T charging current becomes a function of I_{CH} + I_{PL}. $C_{T(min)}$ is found by integrating equation 4 with respect to V_{CT}.

$$C_{T(min)} \cong \left[I_{CH} + \frac{VIN - I_{MAX} \times R_{LOAD} \times \left[1 - e^{\frac{-t}{R_{LOAD} \times C_{LOAD}}}\right]}{R_{PL}}\right] \times \frac{dt}{dV_{CT}} \tag{4}$$

The minimum timing capacitance is found to be:

$$C_{T(min)} = \frac{1}{R_{PL} \times dV_{CT}} \times$$

$$\left[\left(I_{CH} \times R_{PL} + V_{IN} - I_{MAX} \times R_{LOAD}\right) \times t_{START} + V_{IN} \times R_{LOAD} \times C_{LOAD}\right] \tag{5}$$

APPLICATION INFORMATION

selecting other external components

Other external components are necessary for correct operation of the IC. Referring to Figure 11, resistors R_{SENSE}, R_{SS}, R_{DD}, R17, R18, and R19 and the following equations apply:

$$R_{SENSE} = \frac{50\ mV}{I_{FAULT}}$$

$$R_{SS} = \frac{V_{IN} - 5\ V}{I_{DD}}$$

$$R_{DD} = \frac{V_{IN} - 10}{I_{DD}}$$

(R17 + R18 + R19) > 20 kΩ (Current limit out of VREF)

Lastly, use 0.1 µF for the external charge pump capacitors.

soft start

The soft-start circuits in Figure 4a and 4b gradually ramp up the load current on power-up, retry, or if the $\overline{\text{SHTDWN}}$ pin is pulled high. Control circuitry (not shown) turns on Q1 to discharge C1 when $\overline{\text{FLTOUT}}$ or $\overline{\text{SHTDWN}}$ are low (i.e., external power MOSFET is off) so the load current always ramps from zero. The circuit in Figure 4a uses an inexpensive bipolar transistor for Q1 so the component cost is lower than the circuit in Figure 4b.

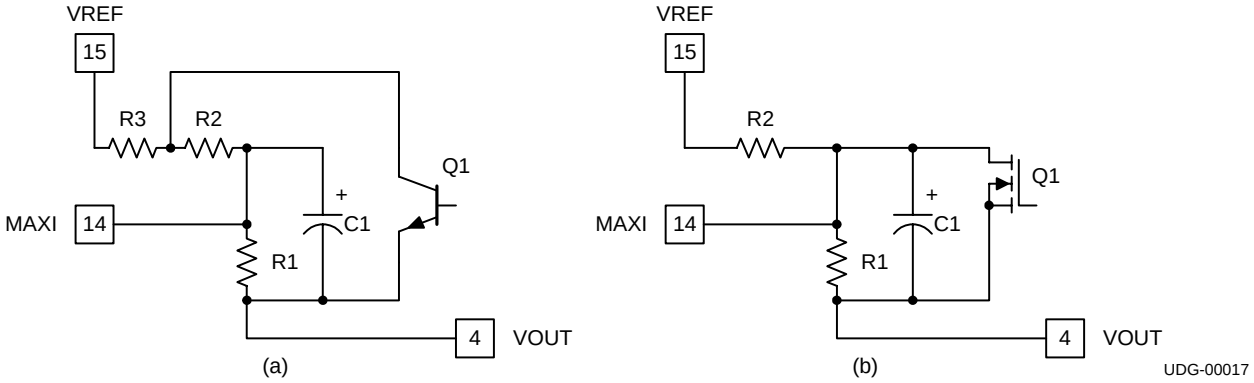


Figure 4. Soft–start Circuits

Soft start minimizes the voltage disturbance on the power bus when a circuit card is inserted into a live back plane. This disturbance could reset a system, which is not desirable when high availability is required. A server is an example of a high availability system.

APPLICATION INFORMATION

soft start (continued)

Soft start is initiated with the $\overline{\text{SHTDWN}}$ pin in Figure 5. The anode of D2 is grounded when the card is in the back plane. R2 limits the $\overline{\text{SHTDWN}}$ pin current to between 60 μA and 500 μA (i.e., 60 μA < 0.65 V / R2 < 500 μA).

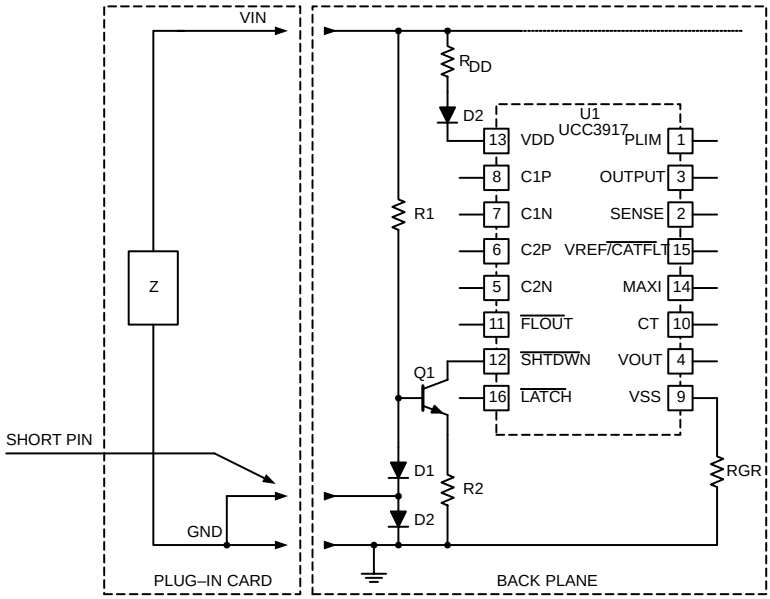


Figure 5. Soft Starting with $\overline{\text{SHTDWN}}$

I/O interface

The UCC3917's $\overline{\text{SHTDWN}}$ and $\overline{\text{LATCH}}$ inputs and $\overline{\text{FLTOUT}}$ output are referenced to VOUT. Level-shifting circuits are needed if the UCC3917 communicates with logic that is referenced to load/system ground.

interfacing to $\overline{\text{LATCH}}$ and $\overline{\text{SHTDWN}}$

Two level shift circuits for $\overline{\text{LATCH}}$ and $\overline{\text{SHTDWN}}$ are shown in Figure 6. The optocoupler (Figure 6a) is simple, but the constant-current sink (Figure 6b) is low cost.

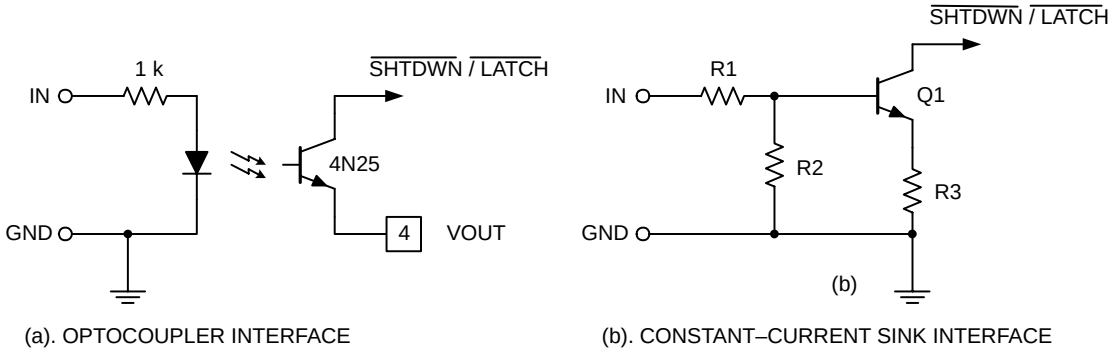


Figure 6. Interfaces

APPLICATION INFORMATION

example #1:

A TTL signal controls the $\overline{\text{LATCH}}$ input of the UCC3917 using the circuit in Figure 6b. Determine the component values if the maximum load voltage is 60 V.

solution:

The assumptions for this analysis are:

$V_{BE} \approx 0.65$ V, $V_{CE(sat)} \approx 0.1$ V, and R1 // R2 << hfe $\times$ R3.

Voltage measurements are with respect to load ground.

Select Q1. The $\overline{\text{LATCH}}$ input is internally pulled up to the charge pump voltage, which is 10 V above the load voltage. Q1 is therefore subjected to 70 V in a 60 V system. A FMMTA06 transistor, with a $V_{CEO(max)}$ of 80 V, is suitable for Q1 in this application.

determine R1-R3.

The interface circuit responds to a TTL input as follows:

Logic “0” input: 0 V < V_{IL} < 0.8 V $\Rightarrow$ 0 μA < I_C < 60 μA and V_C > 1.7 V

Logic “1” input: 2 V < V_{IH} < 5 V $\Rightarrow$ 60 μA < I_C < 500 μA and V_C < 1.7 V

This response establishes the relationship between R1, R2, and R3.

If $V_{IN} = V_{IL(max)} = 0.8$ V then:

(a) Q1 is off $\Rightarrow V_B \approx V_{IL(max)} \times R2 / (R1+R2) < V_{BE} \Rightarrow R1 / R2 > 0.23$

If $V_{IN} = V_{IH(max)} = 5$ V, then:

(a) $I_C = (1.7 \text{ V} – V_{CE(sat)}) / R3 < 500$ μA $\Rightarrow$ R3 > 3.2 kΩ, and

(b) $V_C = (V_{CE(sat)} + V_E) < 1.7 \text{ V} \Rightarrow V_E < 1.6$ V, and

(c) $V_E = (V_B – V_{BE}) < 1.6 \text{ V} \Rightarrow V_B < 2.25$ V, and

(d) $V_B \approx V_{IH\ (max)}) \times R2 / (R1+R2) < 2.25 \text{ V} \Rightarrow R1 / R2 > 1.222$

If $V_{IN} = V_{IH(min)} = 2$ V, then:

(a) $V_B = V_{IH(min)} \times R2 / (R1+R2) \Rightarrow V_B = 2 \text{ V} / (1+R1 / R2)$

(b) $I_C = (V_B – V_{BE}) / R3 > 60$ μA $\Rightarrow R3 < (V_B – V_{BE}) / 60$ μA

In summary, R1, R2, and R3 obey the inequalities:

R1 / R2 > 1.222, and

3.2 kΩ < R3 < $(V_B – 0.65) / 60$ μA, where $V_B = 2 \text{ V} / (1+R1 / R2)$

If R1 / R2 = 1.3, then 3.2 kΩ < R3 < 3.66 kΩ. R1 = 4.64 kΩ for the case where R2 = R3 = 3 kΩ.

The same design can be used to control the UCC3917’s $\overline{\text{SHTDWN}}$ input.

APPLICATION INFORMATION

interfacing to $\overline{\text{FLTOUT}}$

The level shift circuit in Figure 7 is a way to interface to $\overline{\text{FLTOUT}}$. The operation of this circuit and the $\overline{\text{SHTDWN}}$ / $\overline{\text{LATCH}}$ level shift circuit in Figure 6b are similar.

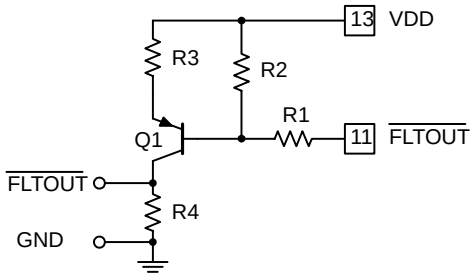


Figure 7. Interfacing to $\overline{\text{FLTOUT}}$

example:

Problem: Design a TTL compatible output level shifter for $\overline{\text{FLTOUT}}$. The maximum system voltage is 60 V.

Solution: Use the level shift circuit in Figure 7.

The $\overline{\text{FLTOUT}}$ output can swing to the charge pump voltage, which is 10 V above the load voltage. In a 60 V application, the collector-emitter of Q1 can be as high as –70 V. A FMMT593 transistor, with a $V_{CEO(max)}$ rating of –100 V, is a suitable choice for Q1.

1. Output saturation voltage constraint.

$V_{C(on)} = V_E + V_{CE(sat)} > 2.4$ V (i.e. TTL output high)

If $V_{C(on)} = 2.6$ V, then $V_E = (2.6\text{ V} + (-0.1\text{ V})) = 2.5$ V.

2. Source current constraint.

$I_C = 100\ \mu A$

3. Calculate the value of R3.

$$R3 = \frac{\left(6\text{ V} - V_E\right)}{I_E} \cong \frac{\left(6\text{ V} - V_E\right)}{I_C}$$

$$R3 = \frac{(6\text{ V} - 2.5\text{ V})}{100\ \mu A} = 35\text{ k}$$

4. Calculate the base voltage.

$V_B = V_E + V_{BE}$

$V_B = (2.5\text{ V} - 0.65\text{ V}) = 1.85$ V

5. The voltage divider formula for R1 and R2 is:

$$\frac{R2}{(R1 + R2)} \times 6\text{ V} \cong \left(6\text{ V} - V_B\right) \quad \text{or} \quad \frac{R1}{R2} = \left(\frac{6\text{ V}}{V_B - 1}\right)$$

APPLICATION INFORMATION

example: (continued)

This equation assumes negligible loading by Q1. That is:

$$\frac{R1}{R2} << hfe \times R3$$

If hfe = 100, then:

$$\frac{R1}{R2} = \left(\frac{6}{1.85 - 1}\right) = 2.24 \text{ and } \frac{R1}{R2} << (100 \times 35\ K) = 3.5\ M$$

If R2 = R3 = 34.8 kΩ, then R1 = 15.4 kΩ

6. The output voltage is set by R4.

$$I_C \times R4 > 2.4\ V$$

$$R4 > \frac{2.4\ V}{100\ \mu A} = 24\ k\Omega. \quad \text{Choose } R4 = 49.9\ k\Omega$$

preloading the output

R_{DD} provides a sneak path for 3mA–11mA of current (e.g., @ 0 V output) to trickle into the load when the power FET is off (see Figure 8).

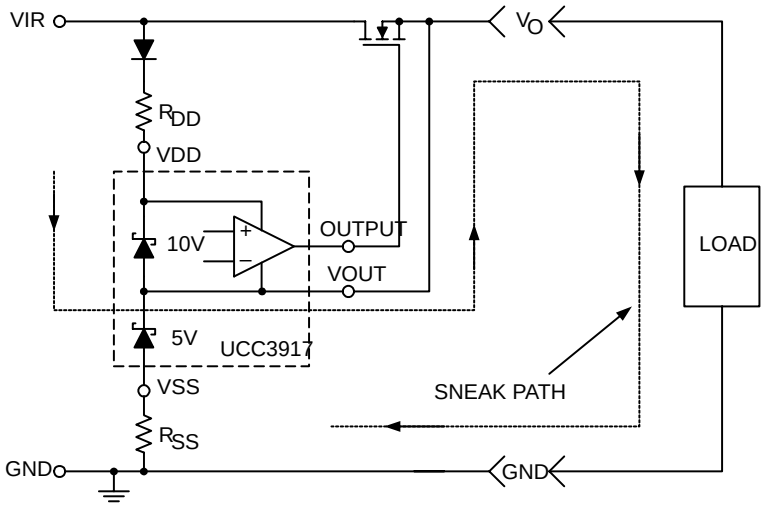


Figure 8. Simplified Schematic Illustrating I_{DD} Sneak Path

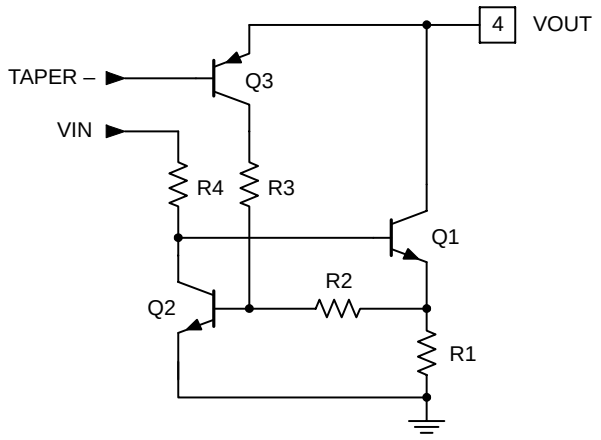
This current causes an unacceptably high output voltage at shutdown if the output is not adequately loaded. In this case, it is necessary to preload the HSPM output to keep the shutdown voltage level acceptable. The preload also insures reliable start-up of the UCC3917 by holding the output voltage low when power is first applied to the HSPM.

A resistor is usually an unacceptable preload because it creates a power dissipation problem when the FET turns on. For example, a 90.9-Ω preload (used to limit the shutdown voltage of a 48-V HSPM to less than 1 V) adds 25-W of power dissipation to the system. In a 100-V system, this dissipation increases to 110 W. The power dissipation overhead increases with the system voltage squared for a resistive preload.

APPLICATION INFORMATION

preloading the output (continued)

The active load in Figure 9 limits the shutdown voltage without creating a power dissipation problem.



UDG-00024

Figure 9. Active Preload

This load is a constant-current sink (i.e., Q3 is off) when the power FET is off. The shutdown voltage is less than 0.85 V if the sink current, set by R1, is greater than 11 mA:

$$I_{SINK(FEToff)} \approx \frac{V_{BE}}{R1} > 11\ mA$$

The power dissipation of Q1 is kept to a minimum when the power FET turns on by tapering the sink current as the load voltage rises:

$$I_{SINK(FETon)} \approx \frac{V_{BE}}{R1} - V_O \times \frac{R2}{(R1 \times R3)}$$

For R1 << R2 << R3

Control circuitry turns on Q3 to activate current tapering. Tapering the current causes the power dissipation of Q1 to peak when the load voltage is:

$$V_O = \frac{V_{BE}}{2} \times \frac{R3}{R2}$$

The power dissipated by Q1 at this voltage is:

$$P_{D(max)Q1} = \left(\frac{V_{BE}}{2}\right)^2 \times \frac{R3}{(R1 \times R2)}$$

In the case of a brownout or if the input voltage rises slowly (e.g., adjustable lab power supply), it is possible for Q1 to dwell in the maximum power dissipation region for a significant time. Limiting the power dissipation of Q1 below its maximum rating insures reliable operation in this case.

APPLICATION INFORMATION

example:

Problem: Design a 14-mA active preload for a 60-V HSPM.

Solution: Set the sink current:

$$R1 = \frac{V_{BE}}{I_{SINK(FEToff)}} = \frac{0.65\ V}{14\ mA} = 46.4\ \Omega$$

Use a BC846B transistor for Q1. This device has a collector breakdown voltage of 65 V and power dissipation rating of 225 mW.

Select R2 & R3 to limit the power dissipation of Q1 to less than 225 mW, say 150 mW:

$$\frac{R3}{R2} = \left(\frac{2}{V_{BE}}\right)^2 \times R1 \times P_{D(max)Q1}$$

$$\frac{R3}{R2} = \left(\frac{2}{0.65\ V}\right)^2 \times 46.4\ \Omega \times 0.15\ W$$

$$\frac{R3}{R2} = 65.9$$

If R2 = 3.01 kΩ, then R3 = 198 kΩ.

The power dissipation of Q1 is shown in Figure 10.

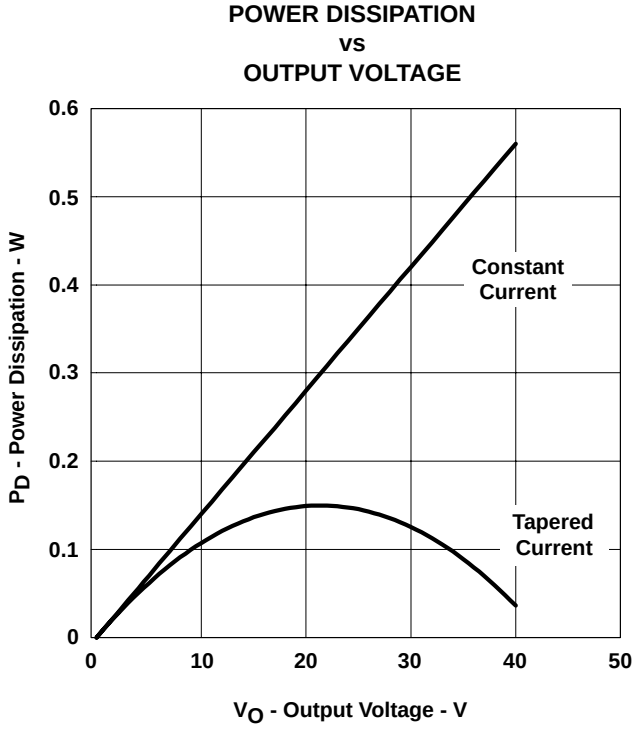


Figure 10.

APPLICATION INFORMATION

protecting the 5-V regulator

The UCC3917's 5-V regulator can overvoltage if VOUT is loaded with less than 11 mA (min) on power up. The overvoltage mechanism is best understood by recognizing that the 5-V Zener diode in the UCC3917 block diagram, is actually a feedback shunt regulator. This regulator turns on when the voltage across the UCC3917's 10-V Zener diode is greater than the UVLO threshold. If VOUT is unloaded and power is applied to the UCC3917, the UVLO threshold cannot be reached and the 5-V regulator impedance is infinite.

Consequently, the entire input voltage appears across the shunt regulator causing it to break down. Clamping its voltage with Zener diode to 5.6 V can protect the regulator. *The Zener diode is unnecessary if the current drawn from VOUT is greater than 11 mA when power is **initially** applied to the UCC3917*.

evaluation circuit example

A 28 V to 60 V @ 1-A HSPM evaluation circuit is shown in Figure 11. Level translation circuitry allows communications with logic referenced to load ground. This circuit is available as a DV3917 Evaluation Board. Contact your local Texas Instruments sales representative for more information.

safety recommendations

Although the UCC3917 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3917 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the power device. The UCC3917 prevents the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot-swap benefits of the device.

APPLICATION INFORMATION

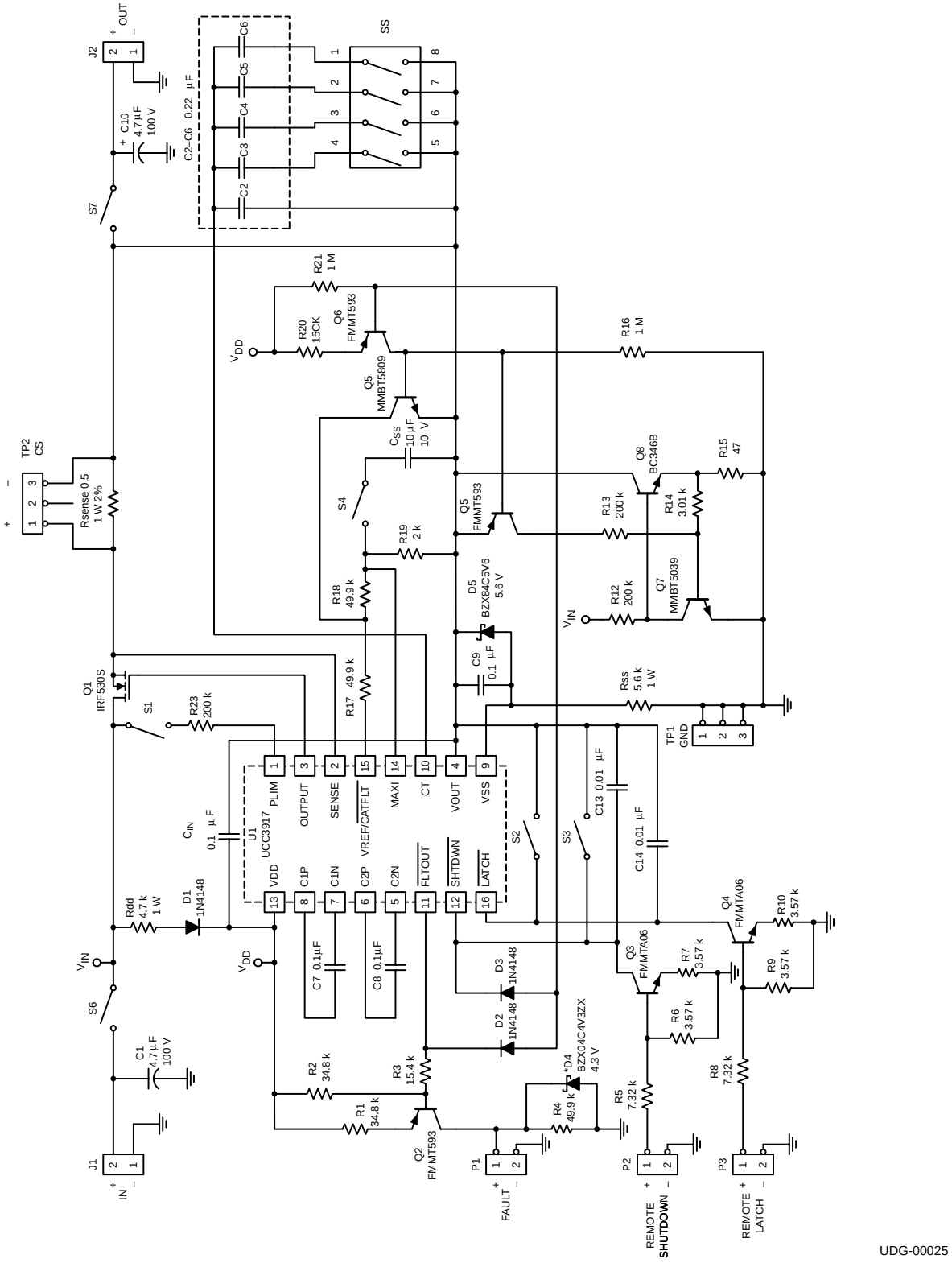


Figure 11. A 28 V to 60 V @ 1-A Positive Floating HSPM Evaluation Circuit Using the UCC3917

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC2917D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2917DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2917DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2917DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC2917N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC2917NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3917D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3917DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3917DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3917DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UCC3917N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UCC3917NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

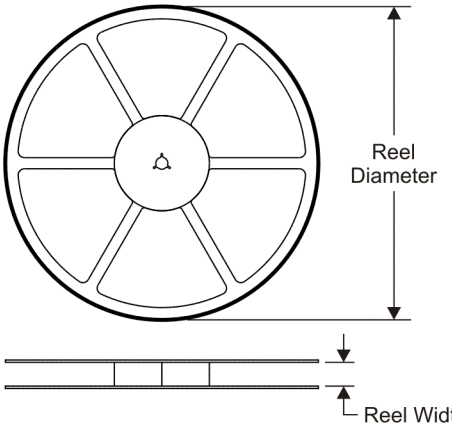
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

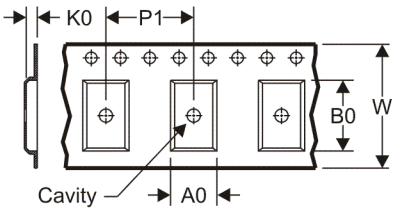
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

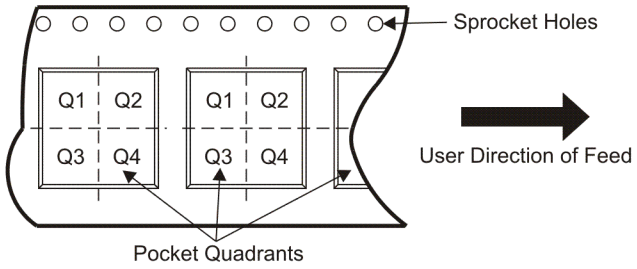


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

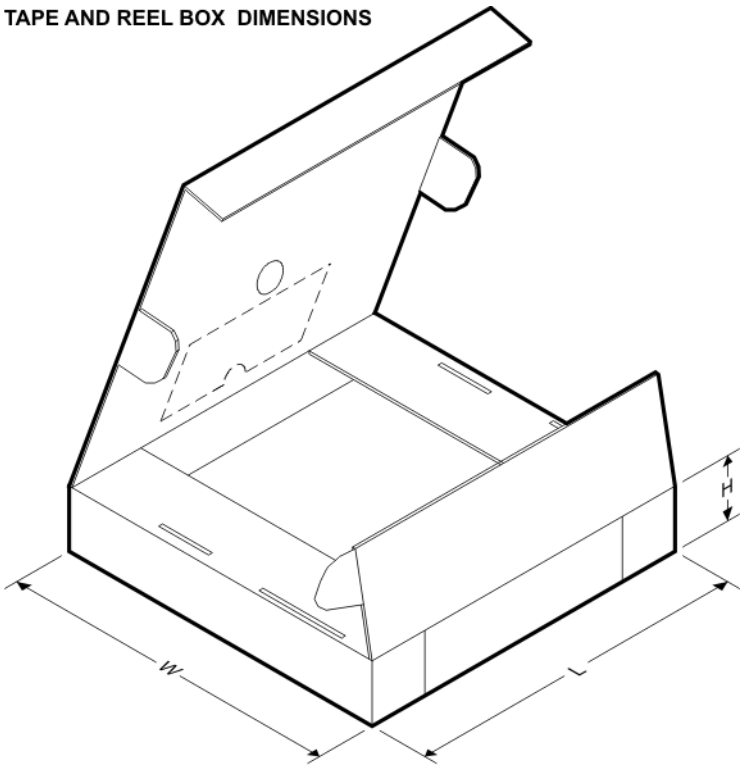
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2917DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3917DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

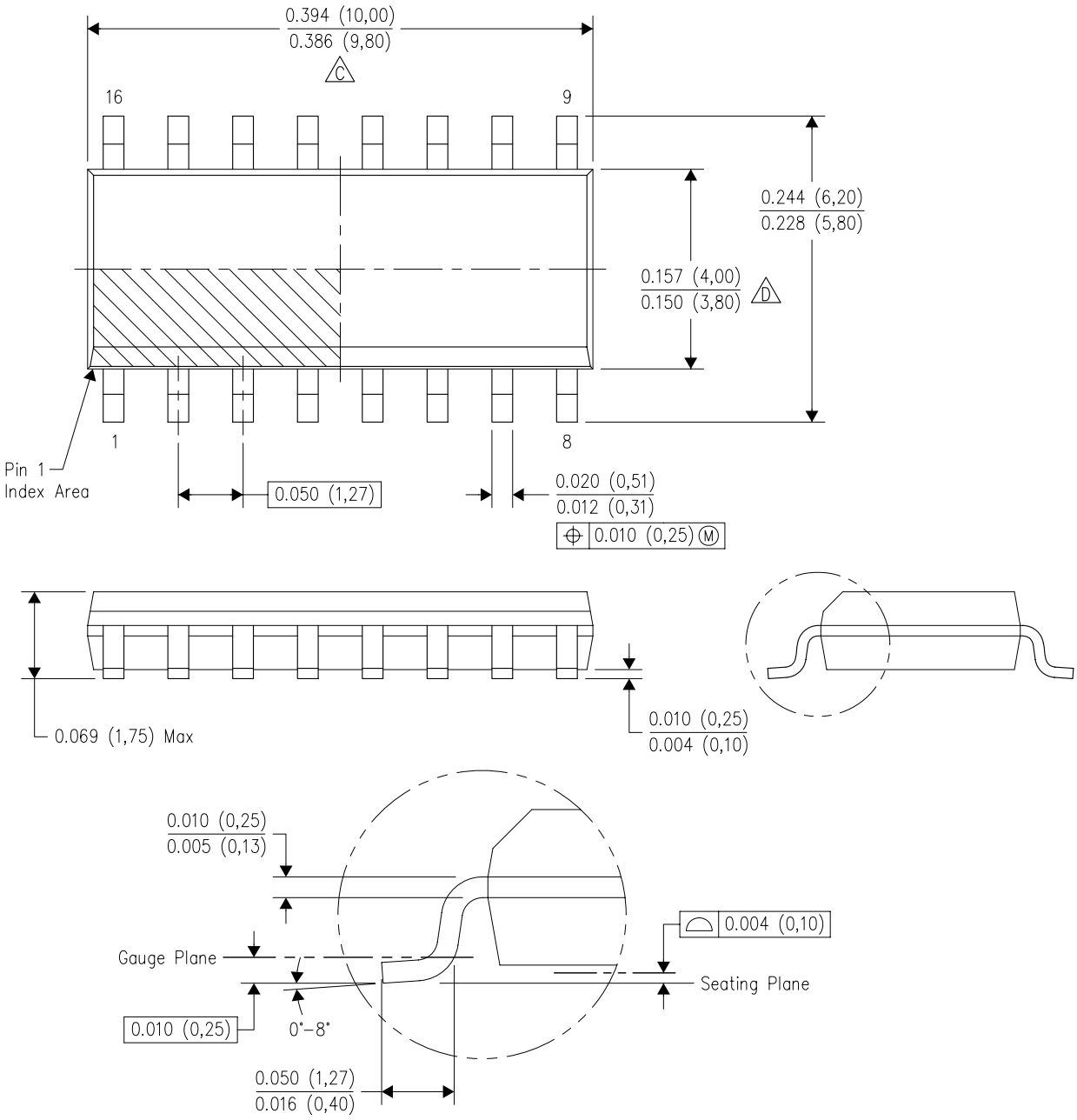
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

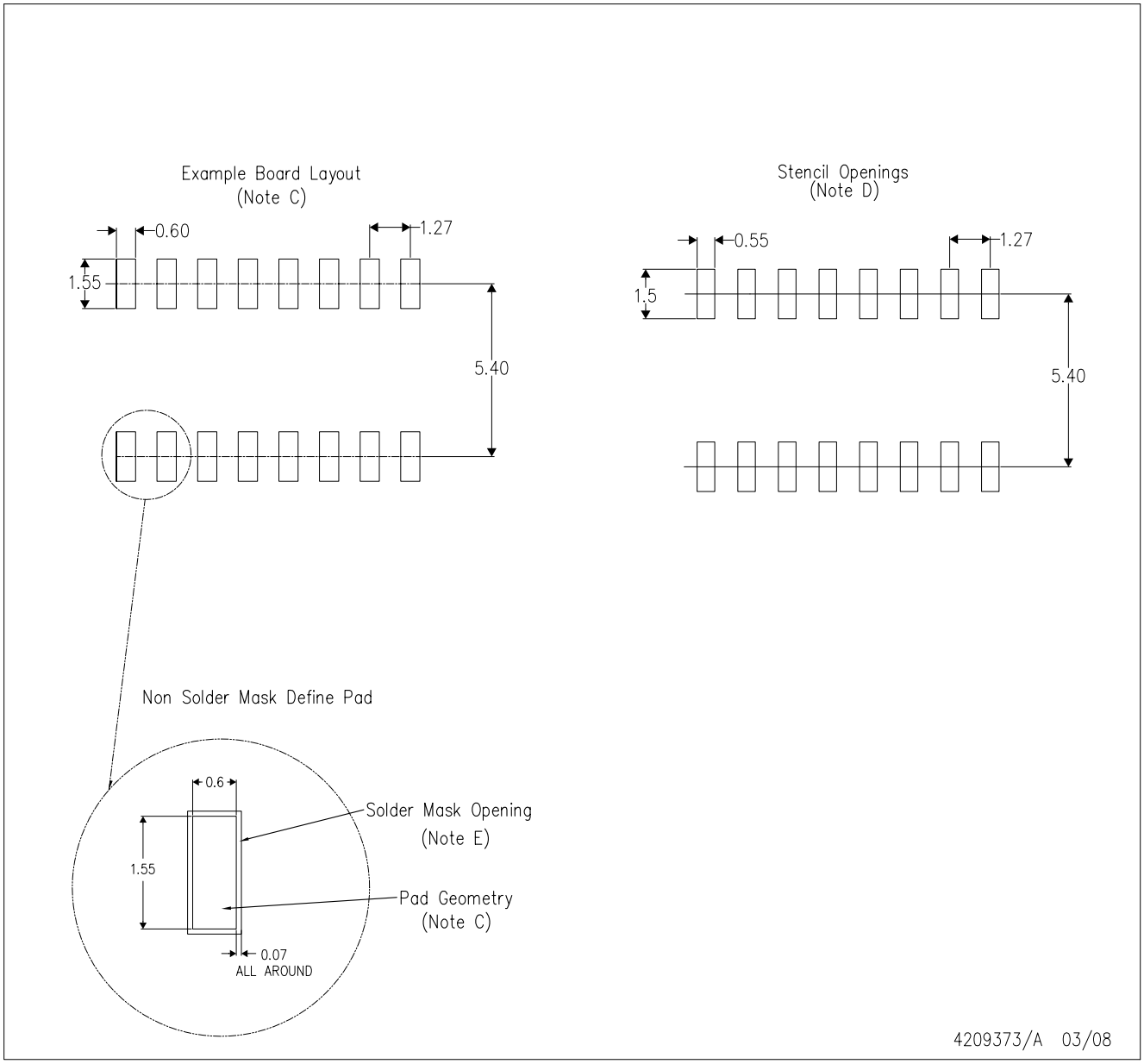
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2917DTR	SOIC	D	16	2500	346.0	346.0	33.0
UCC3917DTR	SOIC	D	16	2500	346.0	346.0	33.0

D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

D(R–PDSO–G16)

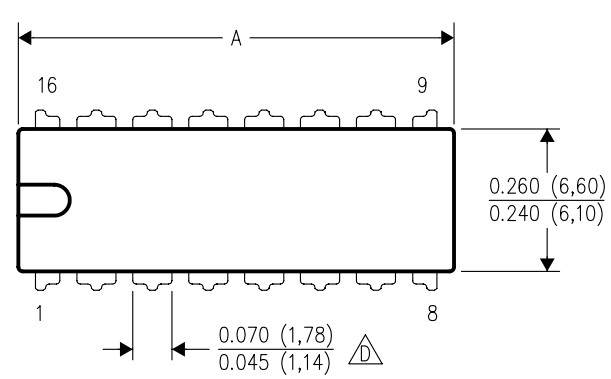


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

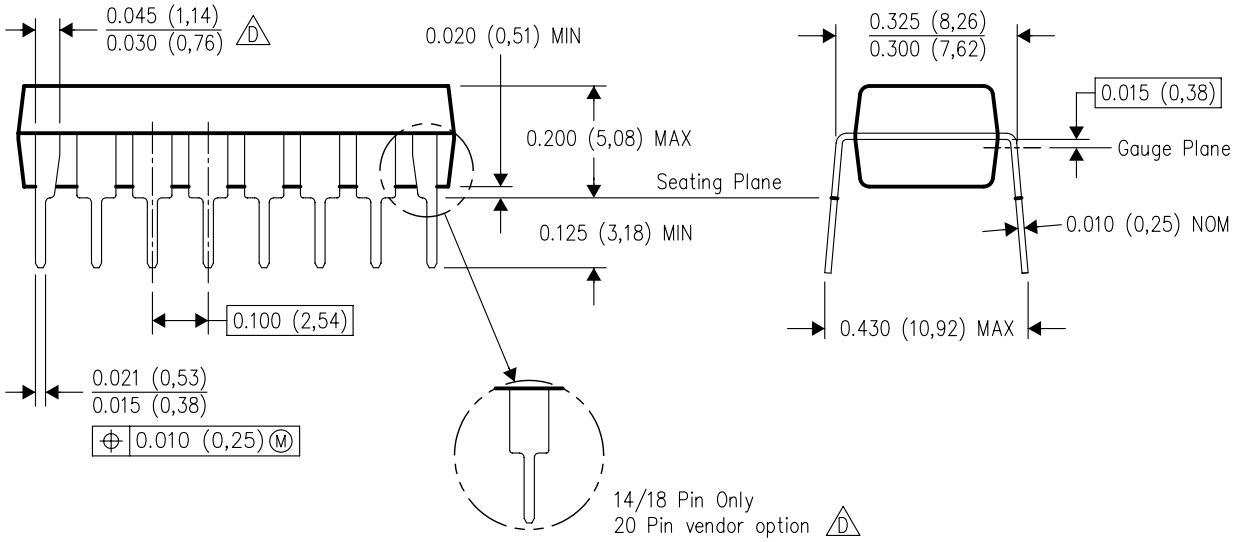
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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