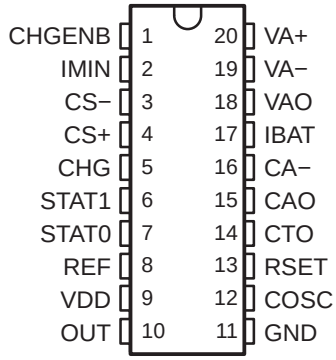
UCC3956
SWITCH-MODE LITHIUM-ION BATTERY CHARGE CONTROLLER

SLUS249B − FEBRUARY 1997 − REVISED DECEMBER 2001

- **Precision 4.1 V Reference (1%)**
- **High-Efficiency Battery Charger Solution**
- **High-Side or Low-Side Switch-Mode Current-Sensing**
- **Average-Current-Mode Control from Trickle to Overcharge**
- **Resistor-Programmable Charge Currents**
- **Internal State Logic Provides Four Charge States**
- **Programmable Overcharge Time**
- **CHG Pin Initiates Charging**
- **Output-Status Bits Report Charge State**

N, DW PACKAGES

(TOP VIEW)



description

The UCC3956 family of switch-mode lithium-ion battery-charger controllers accurately control lithium-ion battery charging with a highly-efficient average-current-control loop. This chip is designed to work as a stand-alone charger controller for a single-cell or multiple-cell battery pack. This chip combines charge-state logic and average-current PWM control circuitry with a 14-bit counter to program the overcharge time. The charge-state logic indicates current- or voltage-control depending on the charge state. The chip includes undervoltage lockout (UVLO) circuitry to ensure sufficient supply voltage is present before output switching starts. Additional circuit blocks include a differential-current-sense amplifier, a 1% voltage reference, voltage- and current-error amplifiers, PWM latch, charge-state decode bits, and a 500-mA output driver.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

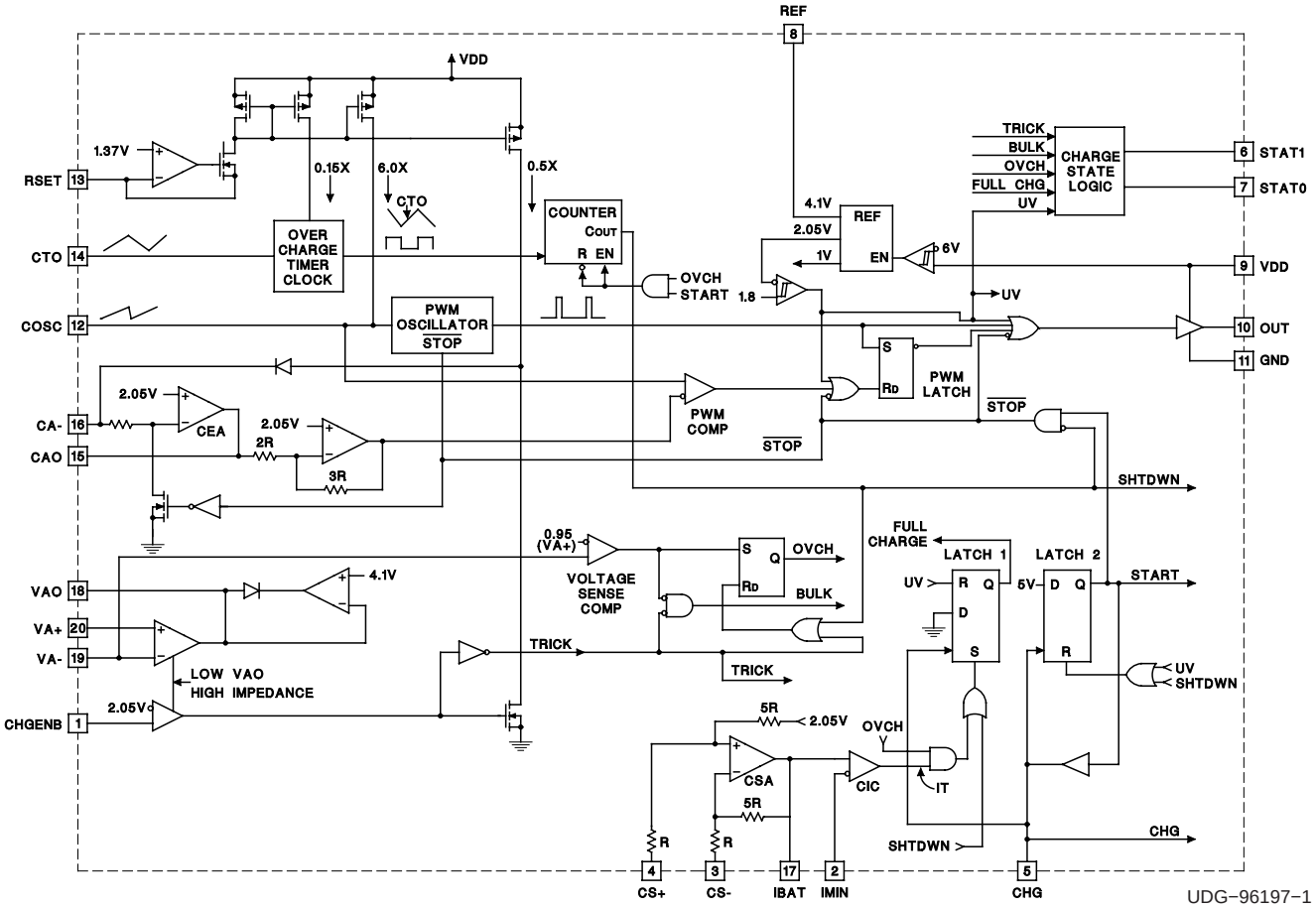
Input voltage (VDD, OUT) . . . . . 20 V
Output current sink
  Continuous . . . . . 120 mA
  Peak . . . . . 600 mA
Output current source
  Continuous . . . . . 120 mA
  Peak . . . . . 600 mA
CS+, CS−
  Voltage . . . . . 0.5 to VDD
  Current with CS+, CS− less than −0.5 . . . . . 50 mA

Remaining pin voltages . . . . . −0.3 V to 6 V
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Operating virtual junction temperature range, T_J . . . . . −55°C to 150°C
Lead temperature (soldering, 10 seconds) . . . . . 300°C
ESD Rating (human body model, HBM) 500V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals. Consult *Packaging Information* section of the *Portable Products Databook* (TI Literature No. SLUD001) for thermal limitations and considerations of packages. All voltages are referenced to GND.

block diagram



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AVAILABLE OPTIONS

T_A	PACKAGED DEVICES	
	(N)	(DW)†
0°C to 70°C	UCC3956N	UCC3956DW

† The DW package is available taped and reeled. Add TR suffix to device type (e.g. UCC3956DWTR) to order quantities of 3000 devices per reel.

electrical characteristics over recommended operating free-air temperature range, T_A = 0°C to 70°C for UCC3956, COSC = 500 pF, RSET = 70 kΩ, CTO = 169 nF, VDD = 12 V, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current Sense Amplifier (CSA) Section						
DC gain	CS– = 0,	CS+ = –50 mV, CS+ = –250 mV	4.9	5.0	5.1	V/V
	CS+ = 0,	CS– = 50 mV, CS– = 250 mV	4.9	5.0	5.1	V/V
Current sense amplifier output (CAO)	CS+ = CS– = 0 V		1.99	2.05	2.11	V
Common mode rejection ratio (CMRR)	V_{CM} = 1.1 V to 18 V,	VDD = 18 V	50	65		dB
Low-level output voltage (VOL)	CS+ = –0.2 V,	CS– = 0.5 V, I_O = 1 mA		0.2	1	V
High-level output voltage (VOH)	CS+ = 0.5 V,	CS– = –0.2 V, I_O = –500 mA	3.7	4.1	4.4	V
Output source current	IBAT = 3 V,	VID = 700 mV	–500			µA
Output sink current	IBAT = 1 V,	VID = –700 mV	500			µA
3dB bandwidth	V_{CM} = 0 V, See Note 2	CS+ − CS– = 100 mV,	0.1	3.0		MHz
Current Error Amplifier (CEA) Section						
Bias current	8 V < V_{DD} < 18 V,	CHGENB = REF		0.1	0.5	µA
Current error amplifier voltage	8 V < V_{DD} < 18 V,	CAO = CA–	1.99	2.05	2.11	V
Open-loop voltage gain (A_{VOL})			60	90		dB
Gain bandwidth	T_J = 25°C,	F = 100 kHz	1	3		MHz
Low-level output voltage (VOL)	I_O = 250 µA,	CA– = 3 V		0.2	1.0	V
High-level output voltage (VOH)	I_O = –1 mA,	CA– = 2 V	3.7	4.1	4.4	V
$I_{CA–}$, $I_{TRCK\_CONTROL}$	V_{CHGENB} = GND		8	10	12	µA
Voltage Error Amplifier (VEA)						
Bias current	Total bias current;	Regulating level		0.5	3.0	µA
Input offset voltage	8 V < V_{DD} < 18 V,	V_{CM} = 4.1 V			10	mV
Open-loop voltage gain (A_{VOL})			60	90		dB
Gain bandwidth	T_J = 25°C,	F = 100 kHz	0.75	3.00		MHz
Low-level output voltage (VOL)	I_O = 500 µA,	VA– = 3.8 V		0.2	1.0	V
High-level output voltage (VOH)	I_O = –500 µA,	VA– = 4.4 V	3.8	4.1	4.3	V
Voltage amplifier output leakage	V_{CHGENB} = GND, VAO = 2.05 V	STAT0 = 0, STAT1 = 0,	–1		1	µA
Pulse Width Modulator Section						
Maximum duty cycle	CAO = 0.5 V		92	96	100	%
Modulator gain	CAO = 1.7 V to 2.1 V		57	64	71	%/V
PWM Oscillator (OSC) Section						
Frequency	7 V < V_{DD} < 18 V		90	100	110	kHz
Overcharge Timer (OCT) Section						
Frequency	7 V < V_{DD} < 18 V	See Note 1	4.65	5.00	5.35	Hz
Reference Section						
Initial accuracy	T_J = 25°C		4.06	4.10	4.14	V
Accuracy	0 < T_J < 70°C,	V_{DD} = 8 V to 18 V	4.05	4.10	4.15	V
	–40°C < T_J < 85°C,	V_{DD} = 8 V to 18 V	4.03	4.10	4.17	V
Load regulation	0 < I_O < 2 mA			3	15	mV
Short circuit I	REF = 0 V		8	20	30	mA

electrical characteristics over recommended operating free-air temperature range, T_A = 0°C to 70°C for UCC3956, COSC = 500 pF, RSET = 70 kΩ, CTO = 169 nF, VDD = 12 V, $T_A = T_J$, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge Enable Comparator (CEC) Section					
Threshold voltage		1.90	2.05	2.15	V
Input bias current		–0.5	–0.2		µA
Voltage Sense Comparator (VSC) Section					
Threshold voltage	Volts below VA+	50	125	200	mV
Charge current comparator (CIC) Section					
Threshold voltage	CS+ = CS– = 0, function of IBAT = 2.05 V	2.00	2.05	2.10	V/V
Input bias current	Total bias current; regulating level	–0.5	–0.2		µA
Output Stage Section					
VOL	I_{OUT} = 10 mA		0.1	0.3	V
VOH, volts below VDD	I_{OUT} = –10 mA		0.1	0.5	V
Rise time	C_{OUT} = 1 nF		30	70	ns
Fall time	C_{OUT} = 1 nF		30	70	ns
STAT0 and STAT1 Open Drain Outputs Section					
Maximum sink current	V_{OUT} = 12 V	15	30		mA
VOL	I_{OUT} = 1 mA		0.1	0.2	V
Charge control (CHG) Section					
Threshold voltage		1.5	1.8	2.1	V
Charge-pin pull-down current	V_{CHG} = 1 V	8	23	40	µA
Undervoltage Lockout Current Section					
Turn−on threshold		6.00	6.50	7.0	V
Hysteresis		75	150	400	mV
Input current					
Quiescent current			5	8	mA
Undervoltage lockout current	VDD = 5 V		0.25	0.75	mA

NOTE 1: 14-bit tuner functionally tested at 500 kHz.
NOTE 2: Ensured by design, not production tested.

pin descriptions

CA–: The inverting input to the current-error amplifier.

CAO: The output of the current-error amplifier and inverting input of the PWM comparator. This pin is driven high during shutdown.

CS–, CS+: The inverting and non-inverting inputs to the current-sense amplifier. This amplifier has a fixed-gain of 5.

CHG: A rising-edge triggered-input pin that indicates charging. Once the internal 14-bit timer has timed out, the chip enters its shutdown charge state. At this point, CHG is pulled low by an internal buffer. Another low-to-high transition is required to reset the timer and restart charging.

CHGENB: The input to a comparator that detects when the battery voltage is low and places the charger in trickle charge. The charge-enable comparator forces the output of the voltage-error amplifier to a high-impedance state while forcing a fixed 10-μA current into the CA– to set the trickle charge.

COSC: The oscillator ramp pin which has a capacitor (COSC) to ground. The ramp oscillates between 0.8 V to 3.2 V and the frequency is determined by:

$$\text{Frequency} = \frac{3.475}{(\text{COSC} + 20\ \text{pF}) \times \text{RSET}} \quad (1)$$

A rising edge on CHG initiates the oscillator.

CTO: The slow oscillator ramp pin, which is used to generate a clock signal for the 14-bit timer to program the overcharge time. A capacitor (tied to ground) is charged and discharged with equal currents at a frequency programmed between 0.75 Hz and 5 Hz. The ramp oscillates between 0.1 V and 3.0 V and the frequency is determined by:

$$\text{Frequency} = \frac{0.06}{(\text{CTO} \times \text{RSET})} \quad (2)$$

The oscillator operates only while in overcharge.

GND: The reference point for the internal reference, all thresholds, and the return for the remainder of the device.

IBAT: The output of the current-sense amplifier.

IMIN: The minimum-charge-current programming pin is provided to program an optional-charge termination in addition to the programmable timer.

OUT: The output of the PWM driver.

REF: The 4.1-V precision reference, which should be bypassed with a 0.1-μF capacitor.

RSET: This pin programs the charge current for the oscillator ramp. The oscillator-charge current is determined by:

$$I_{\text{COSC}} = \frac{1.37\ \text{V}}{\text{RSET}} \quad (3)$$

The trickle-control current ($I_{\text{TRCK\_CONTROL}}$) is determined by:

$$I_{\text{TCK\_CONTROL}} = \frac{0.68\ \text{V}}{\text{RSET}} \quad (4)$$

pin descriptions (continued)

STAT0, STAT1: CMOS open-drain binary-output decode pins indicating the four different charge states. The maximum high-voltage sense comparator.

VA–: The inverting input to the voltage-error amplifier that is used as a battery-sense input. It is also the input to the voltage-sense comparator. The bulk-charge state is completed and overcharge state is initiated when VA– reaches 95% of VA+.

VA+: The non-inverting input to the voltage-error amplifier that is used as the battery-charge reference voltage.

VAO: The output of the voltage-error amplifier. The upper-output clamp of this amplifier is 4.1 V.

VDD: The input voltage of the chip. This chip is operational between 6 V and 18 V and should be bypassed with a 0.1-µF capacitor.

Table 1. Charge State Decode Chart

	STAT1	STAT0	TEST CONDITION
Trickle Charge	0	0	CHGENB < 2.05 V
Bulk Charge	0	1	VA– < 95% VA+, CHGENB > 2.05V
Overcharge	1	0	VA– > 95% VA+, $V_{IBAT} < V_{IMIN}$
Overcharge (Top Off)	1	1	$V_{IBAT} > V_{IMIN}$

APPLICATION INFORMATION

The UCC3956 contains all the necessary control functions for implementing an efficient-switch-mode lithium-ion battery charger. lithium-ion batteries are rapidly becoming the battery of choice for rechargeable portable and laptop products. When compared to NiCd, NiMH, and lead-acid batteries, lithium-ion offers less weight and volume for the same energy. Lithium-ion batteries do not suffer from the memory effect found in NiCd batteries. This effect, caused by not completely discharging and charging a battery, reduces battery capacity over several charge cycles. Because lithium-ion batteries have a high average cell voltage of around 3.6 V, they can often replace two to three nickel-based cells.

The advantages that lithium-ion batteries offer, come at the cost of a wide operating voltage. Near zero capacity, the cell has a typical voltage of 2.5 V. A fully-charged cell has a typical voltage of 4.1 V. Unlike many so called *smart* or *universal* chargers, the UCC3956 is optimized for lithium-ion characteristics. In order to restore capacity quickly, the chip features both constant-current and constant-voltage modes of operation. A programmable overcharge time, provided by the UCC3956 timer, allows the charger to predictably restore 100% capacity to the battery.

charger operation

When CHG is transitioned from a low- to high-logic level, the chip cycles through several charge states. If the battery voltage is severely depleted, the charger begins in a low-current trickle-charge state. When the battery voltage is above a user-set threshold, the charger initiates a constant-current bulk-charge state. Once the battery reaches 95% of it's final voltage, the charger enters an overcharge state. During the overcharge state, the converter transitions from a constant-current to a constant-voltage mode of operation. Figure 2 shows typical current, voltage, and capacity levels of a lithium-ion battery during a complete charge cycle.

APPLICATION INFORMATION

charger operation (continued)

A block diagram of the UCC3956 is shown on the first page of the data sheet, while Figure 1 shows a typical application circuit for a buck-derived switch-mode charger. The UCC3956 can be used for charging a single cell or multiple cells in series. If more than three cells are stacked in series, however, a level-shifting gate-drive may be needed to operate the buck switch. The application circuit charges a 1200-mAh 2-cell stack at a 1C rate.

setting the oscillator frequency

The frequency of operation for the converter is set by picking values for RSET and COSC.

$$f_{OSC} = \frac{3.475}{(COSC + 20pF) \times RSET} \quad (5)$$

The UCC3956 is capable of operating at frequencies higher than 200 kHz. However, the actual operating frequency of the buck converter is ultimately determined by the usual tradeoffs of size, cost and efficiency. The application circuit frequency is set at 100 kHz with COSC = 180 pF and RSET = 162 kΩ.

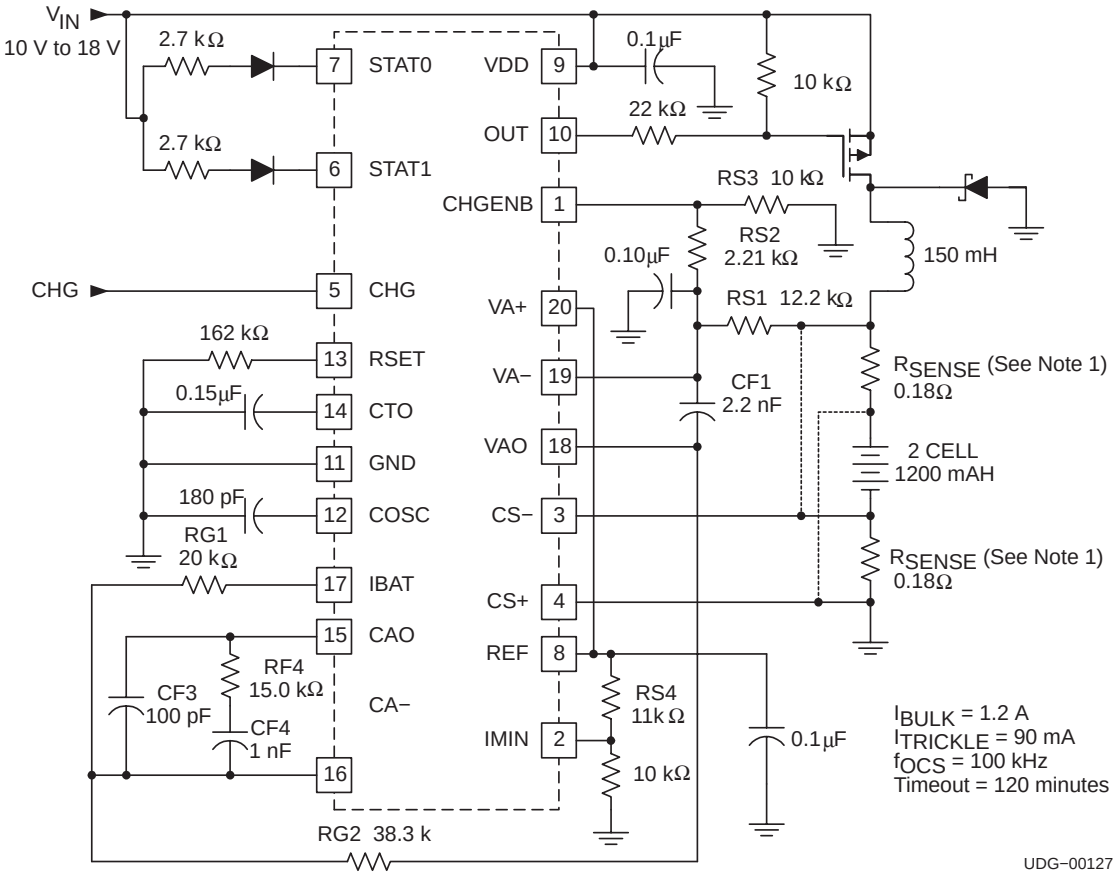

Figure 1. Typical Charge Cycle Levels

NOTE: 1. Either high- or low-side current sensing possible.

APPLICATION INFORMATION

trickle charge state

When the battery's voltage is below a predetermined threshold, the battery is either deeply discharged or has shorted cells. The trickle-charge state offers a low-charging current to bring the battery up above zero capacity. In the case of shorted cells, the trickle-charge state prevents the charger from delivering high currents during this fault condition. Stacking several cells makes the detection of a shorted cell more difficult.

For lithium-ion batteries, the trickle-charge threshold is typically set to a value around 2.5 V per cell (this corresponds to near zero capacity). When the cell voltage is below the threshold, only a trickle current is applied to the battery. The threshold is established by programming CHGENB to 2.05 V when the battery (or stack) voltage is at the threshold. Referring to the application circuit of Figure 1, the trickle-charge voltage threshold is determined by:

$$V_{TRICKLE\_THRESHOLD} = \frac{RS1 + RS2 + RS3}{RS3} \times 2.05 \quad (6)$$

With a trickle threshold of 5 V (for two cells) and setting RS3 to 10 kΩ, (RS1+ RS2) should be approximately 14.4 kΩ.

The applications circuit's trickle-charge current is set to about 7.5% of the bulk-charge current. The current value is set by picking the appropriate value for RG1. Referring to the block diagram and Figure 1, during trickle charge a fixed current (0.68/RSET) flows out of the current amplifier's inverting input and into RG1. The voltage amplifier output is disabled during trickle charge and acts as a high-impedance node. The resulting voltage at the output of the current sense amplifier sets the trickle charge current.

$$I_{TRICKLE} = \frac{RG1}{7.5 \times RSET \times RSENSE} \quad (7)$$

In the application circuit the sense resistor is 0.18 Ω and RSET is 162 kΩ, for a trickle current of about 90 mA a 20-kΩ resistor is selected for RG1.

The converter is typically designed to run in discontinuous-conduction-mode during trickle charge. This allows a reasonably small value of inductance to be used. The average current mode of the UCC3956 provides improved discontinuous-duty-cycle control, when compared to peak-current mode implementations.

In Figure 2, the trickle-charge state corresponds to the time interval between t0 (when CHG is transitioned from low to high) and t1. During the trickle-charge state, STAT0 and STAT1 are logic-level lows. At time t1 the trickle threshold is met, and the charger transitions to the bulk-charge state. In many instances, the battery voltage is initially above the trickle threshold. In this case, the trickle-charge state is not needed.

APPLICATION INFORMATION

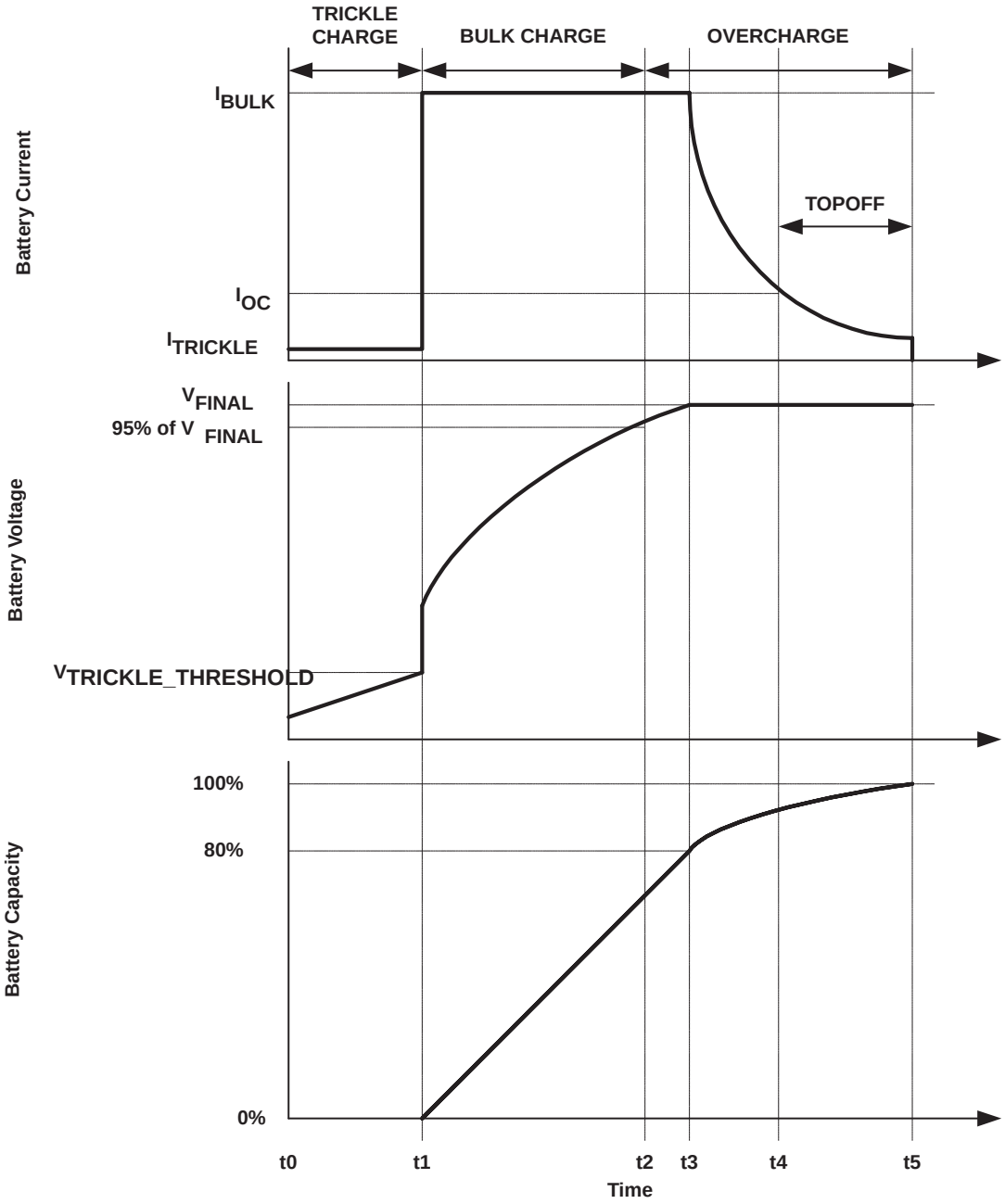

Figure 2. Typical Charge Cycle Levels

APPLICATION INFORMATION

bulk-charge state

As the name implies, the bulk-charge state is responsible for restoring a majority of the charge back into the battery. The bulk-charge current is determined by the C-rate and the capacity of the battery. In the application circuit, two stacked 1200-mAh batteries are charged at a 1C rate. This requires 1.2 A of current during bulk charge. In this case, a fully-discharged battery takes about 60 minutes to reach approximately 80% capacity. Battery packs with a high ESR typically have a shorter bulk period, due to the voltage drop generated by the bulk current and the ESR of the battery.

Both the voltage-sense amplifier and current-sense amplifier are enabled during bulk charge. The voltage amplifier is saturated in this state as the battery voltage is slowly rising, but is not yet high enough to drive the voltage amplifier into regulation. The voltage amplifier output is clamped at a nominal voltage of 4.1 V. The current-sense amplifier is configured so that its output voltage increases with decreasing RSENSE current. RSENSE should be sized such that the output voltage of the current-sense amplifier (V_{IBAT}) is within specification during bulk charge.

$$V_{IBAT(BULK)} = 2.05 - 5 \times IBULK \times RSENSE \quad (8)$$

With 1.2 A of bulk current and the current sense amplifier output set at 1 V, a sense resistor of 0.18 Ω is required. As always, power dissipation and converter efficiency must be considered when choosing RSENSE.

Referring to the feedback diagram of Figure 3, the output of the voltage-sense amplifier and current-sense amplifier are summed at the inverting input of the current amplifier. Assuming that the current-sense amplifier is within regulation, the required value of RG2 can be calculated. The application circuit uses a value of 38.3 kΩ for RG2, setting the bulk current to 1.2 A.

$$RG2 = \frac{2.05 \times RG1}{5 \times IBULK \times RSENSE} \quad (9)$$

Referring to Figure 2, the bulk-charge state corresponds to the interval between t1 and t2. The step-in voltage at time t1 is caused by bulk current flowing into the battery ESR and sense resistor. In the bulk-charge state, STAT0 is a logic-level high and STAT1 is a logic-level low.

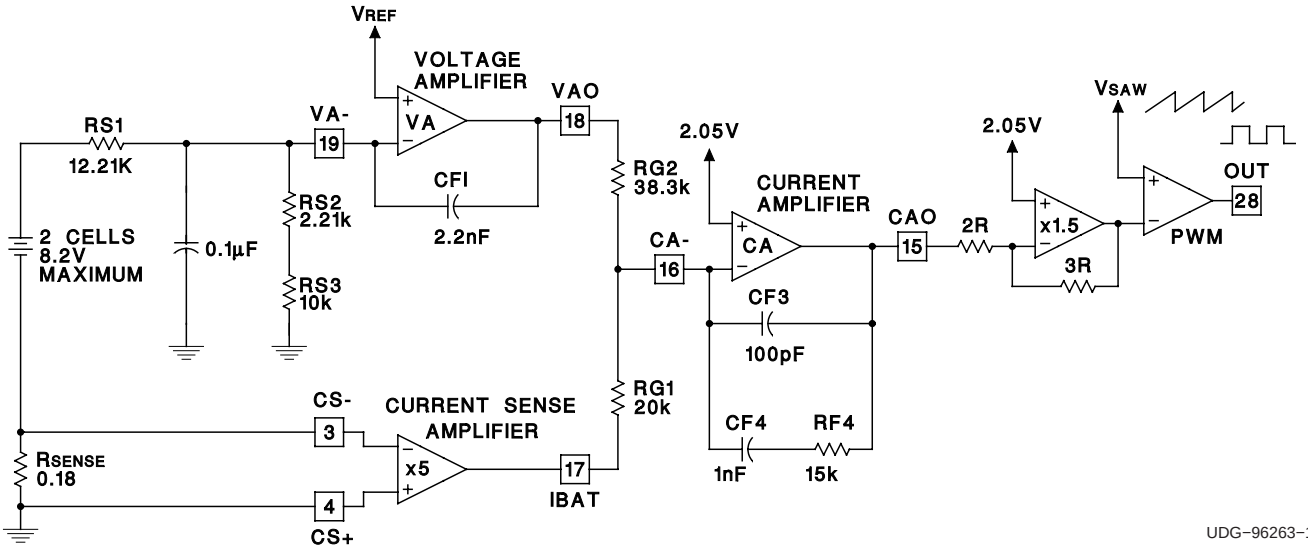

Figure 3. Typical Charge Cycle Levels

APPLICATION INFORMATION

overcharge state

The overcharge state of the converter starts when the battery reaches 95% of its final voltage (time t2 of Figure 2). The overcharge state is initiated when the voltage at the inverting input of the voltage amplifier is 95% of the non-inverting-input voltage. Using 95% rather than 100% of the final battery voltage assures that the overcharge timer is always set before the battery current tapers off. At the beginning of overcharge state, STAT0 indicates a logic-level low and STAT1 indicates a logic-level high.

In the application circuit of Figure 1, the voltage at which overcharge is initiated is set by resistors RS1, RS2 and RS3. These resistors are also used to set the trickle-charge threshold. A 0.1-µF decoupling capacitor is added to this node as a filter. The battery (or stack) voltage that initiates the overcharge state is:

$$\text{VOC\_THRESHOLD} = 0.95 \times \frac{\text{RS1} + \text{RS2} + \text{RS3}}{\text{RS2} + \text{RS3}} \times 4.1 \quad (10)$$

For a single-cell stack, RS1 should be 0 Ω. This results in a final battery voltage of 4.1 V. It is important not to charge a lithium-ion battery above 4.2 V. When charging a battery stack, RS1 should be selected to properly set the final-stack voltage. In the application circuit, RS1 is selected to be 12.21 kΩ and RS2 is selected to be 2.21 kΩ. This sets the overcharge level at 8.2 V, while setting the trickle-charge threshold to about 5 V.

The battery voltage at the beginning of the overcharge state may not correspond to the voltage amplifier coming out of saturation. Therefore, bulk current may continue in the battery during the initial portion of the overcharge state (see Figure 2). When the voltage amplifier comes into regulation, the amplifier's output voltage begins to decrease. The current-sense amplifier's output voltage needs to increase in order for the current amplifier's inverting input to remain at 2.05 V. This translates into a decreasing battery current. The battery current continues to decrease as the battery approaches 100% capacity.

Although the bulk-charge state restores a majority of the capacity to the battery, the overcharge state typically takes a majority of the charge-cycle time. The bulk-charge state usually takes one-third of the total charge time, while the overcharge state takes the remaining two-thirds. Different methods are used to terminate the charge of lithium-ion batteries. Many chargers use a current threshold to terminate charge. While this method is simple to implement, the current tail near the end of charge is often quite flat (see Figure 2). To make matters worse, the current level versus battery capacity may differ from cell to cell. This makes it difficult to accurately terminate at 100% capacity. In order to avoid the possibility of overcharging the battery, the design may require termination at a higher current level (before 100% capacity is reached). A more predictable method of charge termination is to use a fixed overcharge time.

The UCC3956 provides current-level detection as well as a timer. In a typical design, the current-level detection is used to give an indication of near-full charge. As shown in Figure 2 this occurs at time t4. This indication is useful since the time to charge from t4 to t5 may be quite long. Since lithium-ion batteries have no memory effect, there is little reason to have the user wait for the battery to be 100% charged. If the battery is not taken from the charger at time t4, the charger continues charging. The timer expires and the charge cycle terminates at time t5.

A typical value used to indicate near-full charge is one−tenth of the bulk current value. This current level is established by setting the appropriate voltage on IMIN. IMIN is tied to an internal comparator along with the output of the current sense amplifier. When the current sense amplifier voltage becomes greater than the voltage on IMIN, the internal state machine indicates near full charge by setting STAT0 and STAT1 to logic level highs. In the application circuit of Figure 1, resistors RS4 and RS5 determine the voltage at IMIN. With RS4 at 11 kΩ and RS5 at 10 kΩ, near full charge is indicated at 120 mA.

$$V_{IMIN} = 4.1 \times \frac{\text{RS5}}{(\text{RS4} + \text{RS5})} \quad (11)$$

$$I_{NEAR\_FULL} = \frac{2.05 - V_{IMIN}}{5 \times R_{SENSE}} \quad (12)$$

The UCC3956 timer has a 14-bit counter that allows long overcharge times with reasonable component values. As previously stated, the charger continues charging the battery until the timer expires (unless the battery is pulled from the charger). As seen in Figure 2, the timer starts at time t2 and expires at time t5. The frequency of the timer can be determined as follows:

$$f_{TIMER} = \frac{0.06}{RSET \times CTO} \quad (13)$$

With a 14-bit counter the time-out period in minutes becomes:

$$TIMEOUT = 4550 \times CTO \times RSET \quad (14)$$

In the application circuit, a value of 0.15 μF is used for CTO to give 120 minutes of overcharge (more than twice the bulk-charge time). When the timer expires, CHG is pulled low by an internal buffer and the charge cycle terminates. If tied to a bidirectional port, CHG can be read by a microprocessor.

inductor sizing

For good efficiency, the inductor should be sized to give continuous current in the bulk-charge state. For a buck converter, duty-cycle in continuous mode is given by:

$$D = \frac{V_{BATTERY} + V_{SCHOTTKY}}{V_{INPUT} + V_{SCHOTTKY}} \quad (15)$$

Allowing a 25% ripple in the bulk current yields a reasonable value of inductance. The inductor value can be calculated as follows:

$$L = \frac{4 \times \left(V_{INPUT} - V_{BAT}\right) \times D}{IBULK \times f_{OSC}} \quad (16)$$

A 150-μH inductor is used in the application circuit.

current control loop

The UCC3956 features an outer-voltage loop and an inner-average current loop. The virtues of average-current mode control are well documented in Reference [1]. A simplified block diagram of the feedback elements is provided in Figure 3. The network for the current amplifier can be as simple as a single capacitor, providing a dominant-pole response, which may be adequate for a battery-charger application. The current-amplifier network of shown in Figure 3 provides improved transient performance. The component values for CF3, CF4, and RF4 are selected to give a constant gain from approximately $f_{OSC}/10$ to f_{OSC}. At frequencies below $f_{OSC}/10$, the network gain increases at 20 dB/decade, giving a high dc gain. The network attenuates at 20 dB/decade above the switching frequency, giving noise immunity.

A feedback design that optimizes transient response has the amplified inductor current down-slope approach the PWM saw-tooth slope [1]. This occurs by designing the total-loop gain to cross unity at one-third to one-sixth of the switching frequency. The applications circuit is designed to cross unity gain at one-tenth of the switching frequency (10 kHz), with a 12 V nominal input. The power stage small-signal gain can be approximated by:

$$G_{POWER\_STAGE} = \frac{VIN \times RSENSE}{SL + RSENSE + ESL} \quad (17)$$

APPLICATION INFORMATION

current control loop (continued)

Referring to Figure 3, the current-sense amplifier provides a gain of 5 db, an inverting stage adds a gain of 1.5 db, and the modulator has a gain of 0.64 db; adding a fixed gain of 4.8 db to the power stage. The current amplifier's gain between $f_{OSC}/10$ and f_{OSC} is equal to RF4 divided by the parallel combination of RG1 and RG2 times the resistive divider RG2/(RG1+RG2), simplifying to:

$$GCA = \frac{RF4}{RG1} \tag{18}$$

RF4 is selected to be 15 kΩ, resulting in a 10-kHz crossover frequency. Once RF4 is determined, CF3 and CF4 can be selected to give corner frequencies at $f_{OSC}/10$ and f_{OSC} respectively.

$$CF3 = \frac{1}{2 \times \pi \times f_{OSC} \times RF4} \tag{19}$$

$$CF4 = \frac{10}{2 \times \pi \times f_{OSC} \times RF4} \tag{20}$$

In the applications circuit, a value of 100 pF is used for CF3 and 1.0 nF is used for CF4. Figure 4 shows the power-stage gain and feedback-network gain for the current loop. Figure 5 shows the total open-loop gain and phase.

adding the voltage-control loop

The voltage loop begins to regulate during the overcharge period of operation. The output of the voltage amplifier begins to decrease, demanding less current to the battery. With the current loop closed, the power-stage gain of the voltage loop is equal to $1 \Big/ \left(5 \times R_{SENSE}\right)$ out to the crossover frequency (10 kHz). In order to avoid interactions with the current loop, the voltage loop will cross unity at 2 kHz. The voltage loop is attenuated by the divider $RG1/(RG1 + RG2)$. A single pole network is added to the voltage amplifier, giving a high gain at dc. Referring to Figure 3, the voltage-amplifier gain is equal to the impedance of CF1 divided by RS1. A 2.2-nF capacitor gives a total-crossover frequency near 2 kHz. Figure 6 shows the gain of the power and feedback stages for the voltage loop. Figure 7 shows the total gain and phase of the voltage loop.

TYPICAL CHARACTERISTICS

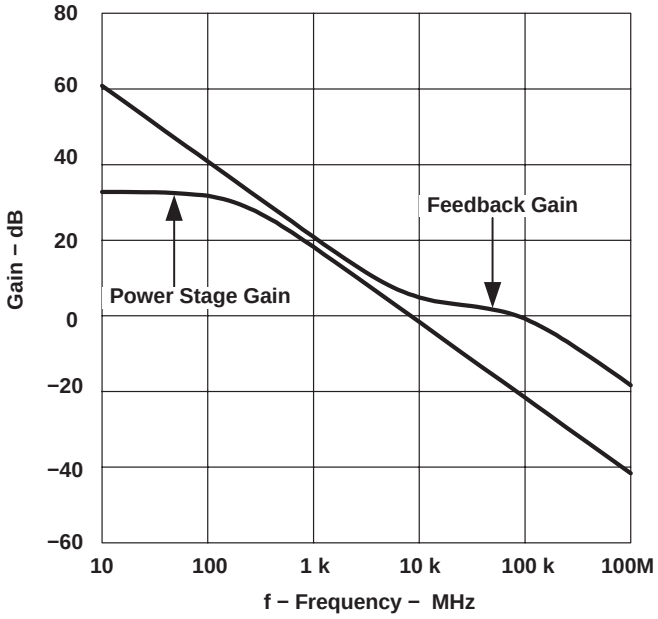

Figure 4

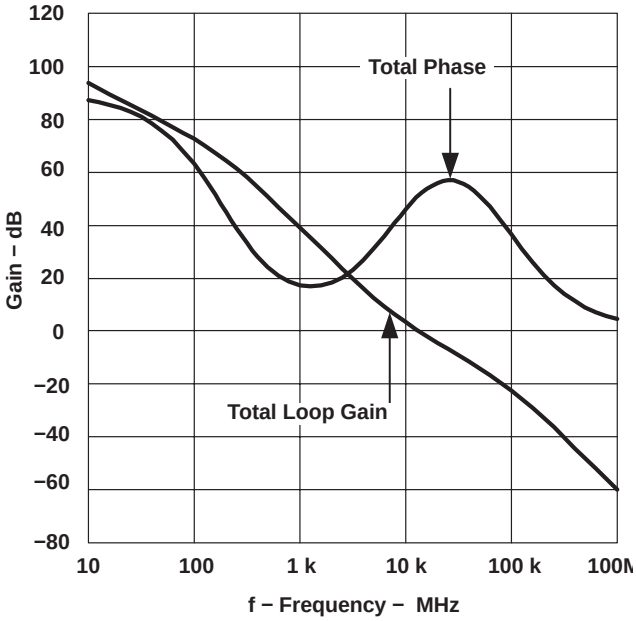

Figure 5

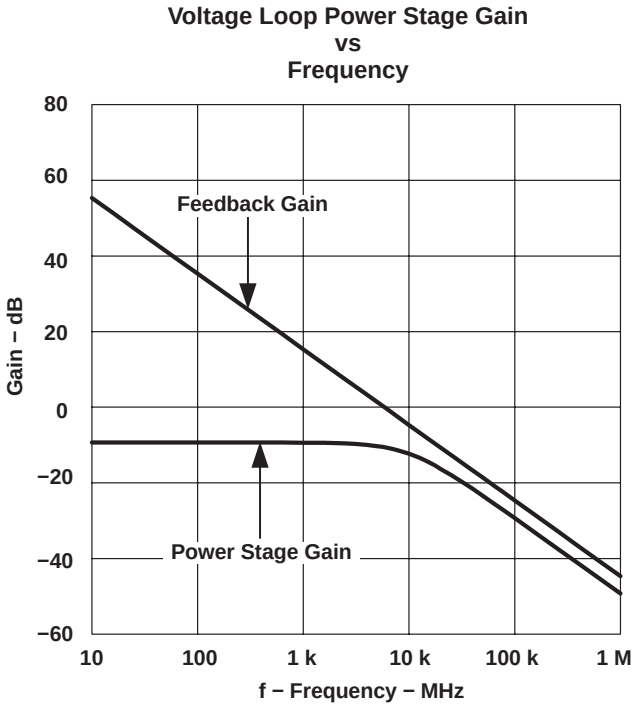

Figure 6

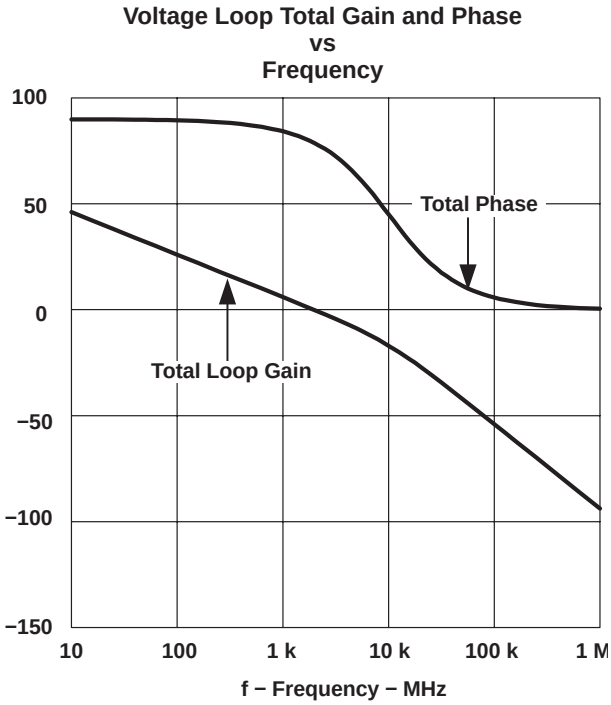

Figure 7

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