CMOS Digital Integrated Circuits Silicon Monolithic

# 74HC4538D

## 1. Functional Description

- Dual Monostable Multivibrator

## 2. General

The 74HC4538D is a high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate $C^2MOS$ technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

There are two trigger inputs, A input (positive edge input), and $\overline{B}$ input (negative edge input). These inputs are valid for a slow rise/fall time signal ($t_r = t_f = 1$ s) as they are schmitt trigger inputs.

After triggering, the output stays in a MONOSTABLE state for the time period determined by the external resistor and capacitor ($R_X$, $C_X$). A low level at $\overline{CD}$ input breaks this STABLE STATE. In the MONOSTABLE state, if a new trigger is applied, it makes the MONOSTABLE period longer (retrigger mode).

Limitations for $C_X$ and $R_X$ are as follows:

External capacitor $C_X$.....No limitation

External resistor $R_X$.....$V_{CC}$ = 2.0 V more than 5 kΩ

$V_{CC}$ = 3.0 V more than 1 kΩ

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

## 3. Features (Note)

(1) High speed: tpd = 25 ns (typ.) at $V_{CC}$ = 5 V

(2) Low power dissipation:

Standby state: $I_{CC}$ = 4.0 μA (max) at $T_a$ = 25 °C

Active state: $I_{CC}$ = 350 μA (max) at $T_a$ = 25 °C

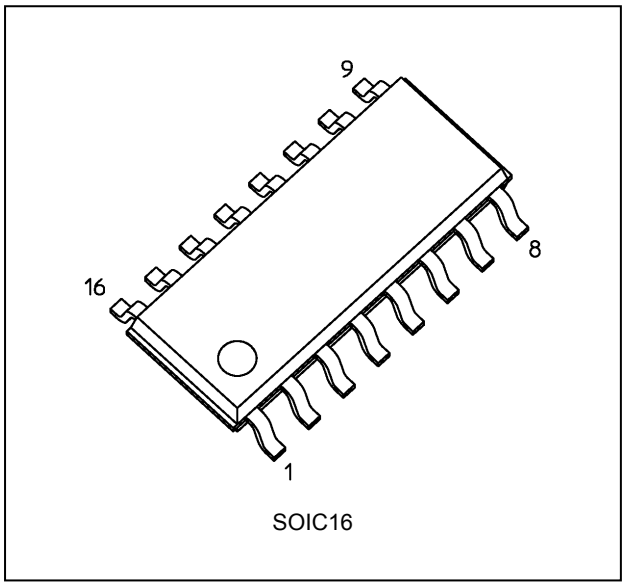
(3) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$

(4) Wide operating voltage range: $V_{CC(opr)}$ = 2.0 to 6.0 V

Note: In the case of using only one circuit, $\overline{CD}$ should be tied to GND, T1 · T2 · Q · $\overline{Q}$ should be tied to OPEN, the other inputs should be tied to $V_{CC}$ or GND.

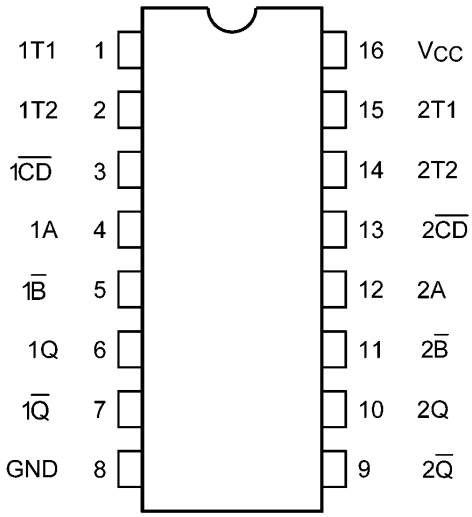
Start of commercial production
2016-05

## 4. Packaging



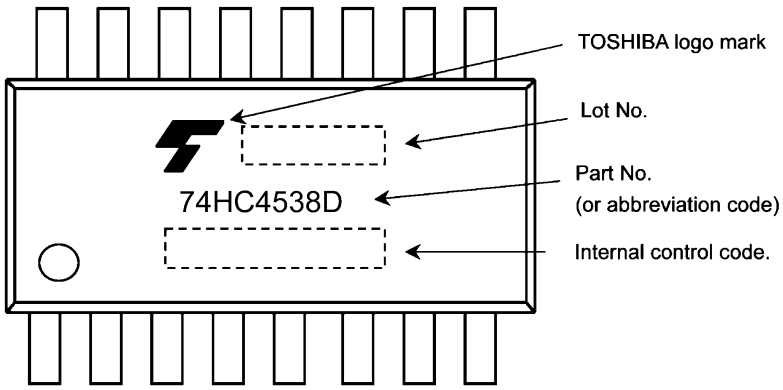

SOIC16

## 5. Pin Assignment

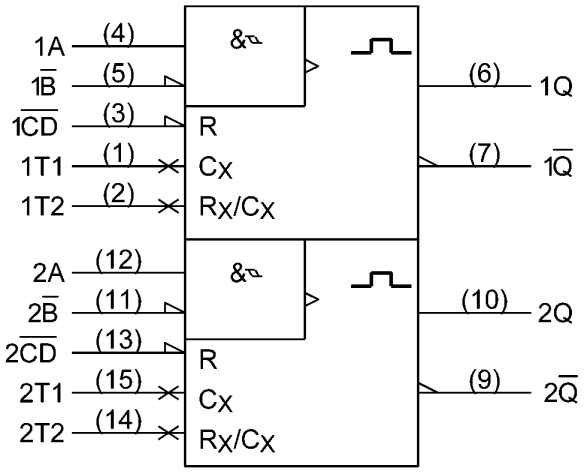



(top view)

## 6. Marking



## 7. IEC Logic Symbol

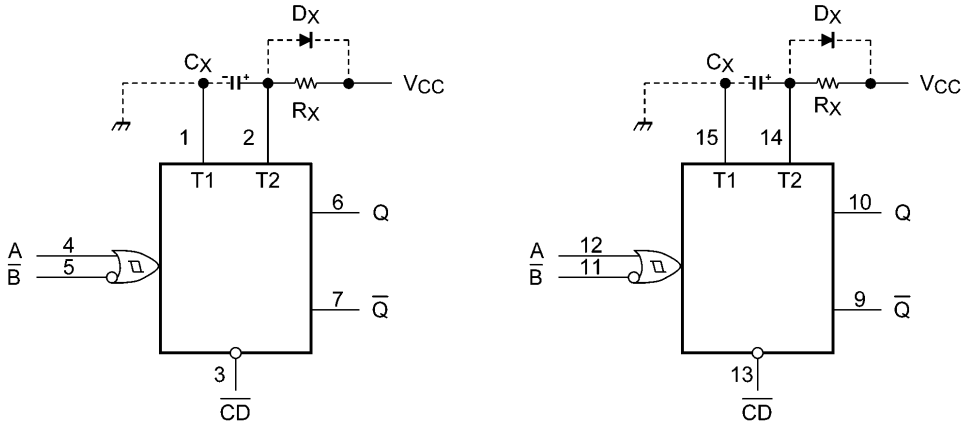



## 8. Truth Table

| Inputs | | | Outputs | | Note |
|---|---|---|---|---|---|
| A | $\overline{B}$ | $\overline{CD}$ | Q | $\overline{Q}$ | |
| ↑ | H | H | ⊓ | ⊔ | Output Enable |
| X | L | H | L | H | Inhibit |
| H | X | H | L | H | Inhibit |
| L | ↓ | H | ⊓ | ⊔ | Output Enable |
| X | X | L | L | H | Reset |

X: Don't care

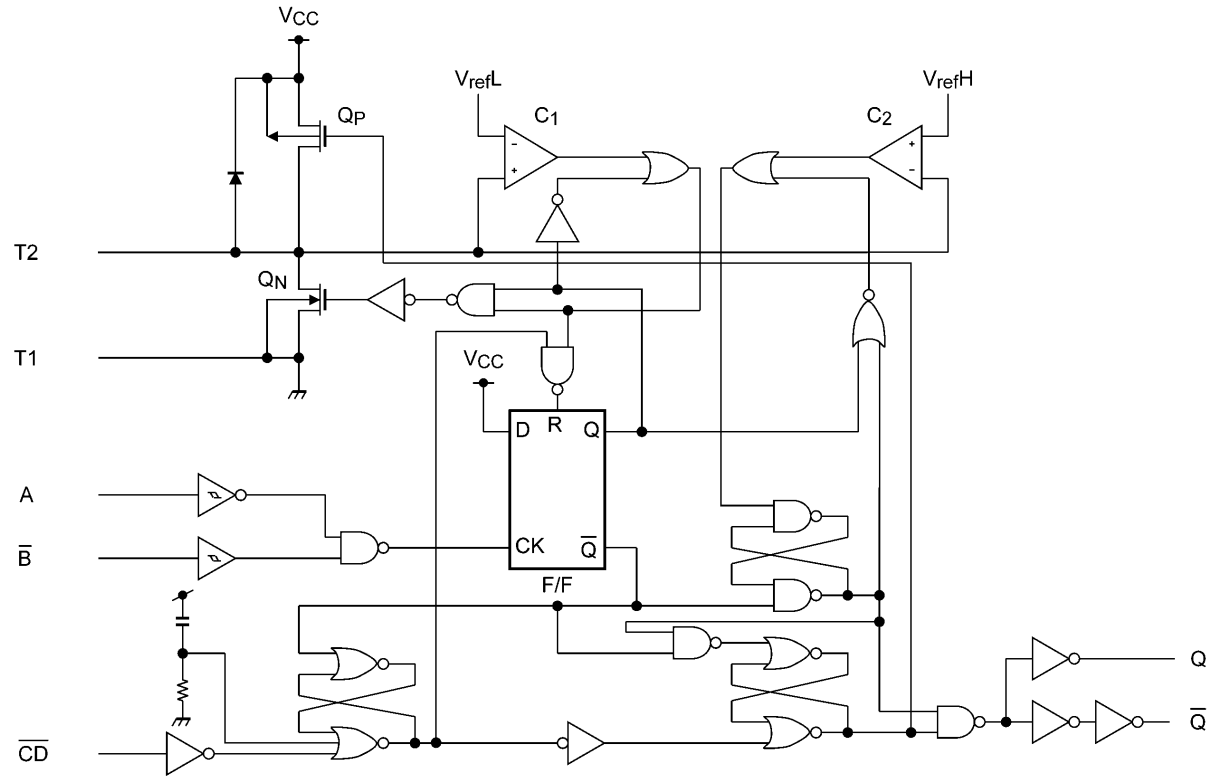
## 9. Block Diagram



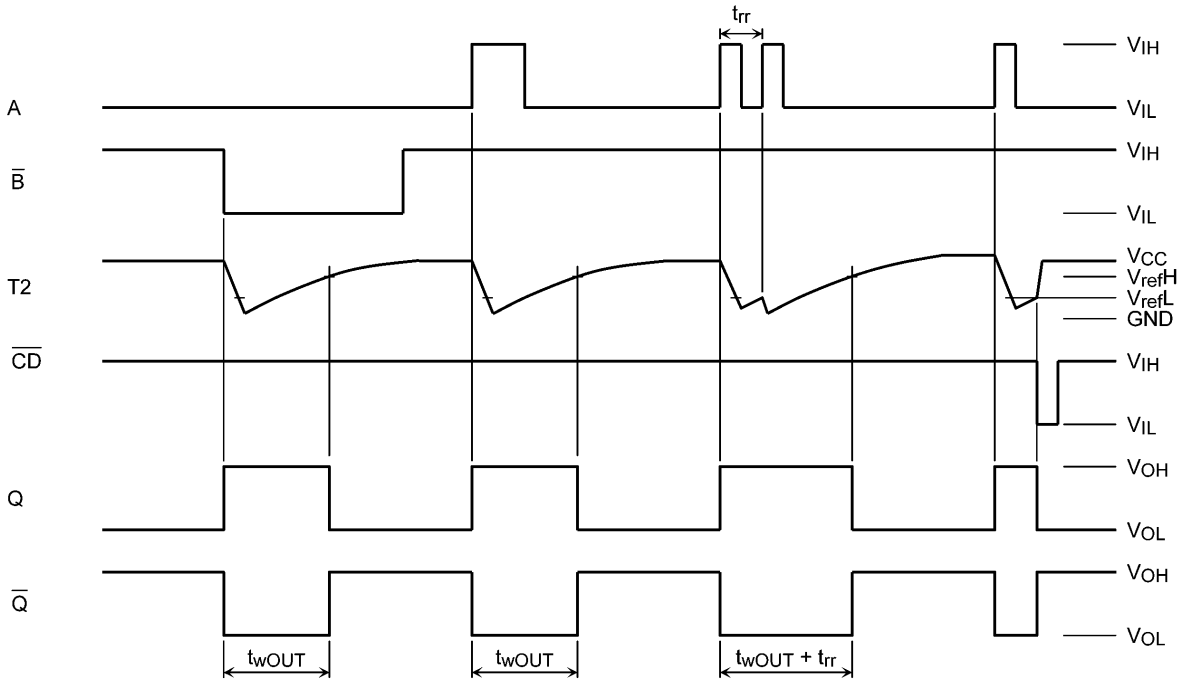

(1) $C_X$, $R_X$, $D_X$ are external
Capacitor, resistor, and diode, respectively.

(2) External clamping diode, $D_X$;
The external capacitor is charged to $V_{CC}$ level in the wait state, i.e. when no trigger is applied. Supply voltage is turned off and $C_X$ is discharged mainly through the internal (parasitic) diode. If $C_X$ is sufficiently large and $V_{CC}$ drops rapidly, there will be some possibility of damaging the IC by rush current or latch-up. If the capacitance of the supply voltage filter is large enough and $V_{CC}$ drops slowly, the rush current is automatically limited and damage to the IC is avoided.
The maximum value of forward current through the parasitic diode is ±20 mA.
In the case of a large $C_X$, the limitation of fall time of the supply voltage is determined as follows:
$t_f \geq (V_{CC} - 0.7)\ C_X/20$ mA
($t_f$ is the time from the voltage supply turning off to the level of supply voltage reaching 0.4 $V_{CC}$.)
In the care of a system that does not satisfy the above condition, an external clamping diode is needed to protect the IC from rush current.

## 10. System Diagram




## 11. Timing Chart



## 12. Functional Description

(1) Stand-by state

The external capacitor is fully charge to $V_{CC}$ in the stand-by state. That means, before triggering, $Q_P$ and $Q_N$ transistors which are connected to the T2 node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies stop their operation. The total supply current is only leakage current.

(2) Trigger operation

Trigger operation is effective in either of the following two cases. One is the condition where the A input is low, and the $\overline{B}$ input has a falling signal. The other, where the $\overline{B}$ input is high, and the A input has a rising signal.

After trigger becomes effective, comparators $C_1$ and $C_2$ start operating, and $Q_N$ is turned on. The external capacitor discharges through $Q_N$. The voltage level at the T2 node drops. If the T2 voltage level falls to the internal reference voltage $V_{ref}L$, the output of $C_1$ becomes low. The flip-flop is then reset and $Q_N$ turns off. At that moment $C_1$ stops but $C_2$ continues operating.

After $Q_N$ turns off, the voltage at T2 start rising at a rate determined by the time constant of external capacitor $C_X$ and resistor $R_X$.

After the triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of T2 changes from falling to rising. When T2 reaches the internal reference voltage $V_{ref}H$, the output of $C_2$ becomes low, the output Q goes low and $C_2$ stops its operation. That means, after triggering, when the voltage level of T2 reaches $V_{ref}H$, the IC returns to its MONOSTABLE state.

In the case of large value of $C_X$ and $R_X$, and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse, ($t_{wOUT}$), is as follows:

$$t_{wOUT} = 0.7 \times C_X \times R_X$$

(3) Retrigger operation

When another new trigger is applied to input A or $\overline{B}$ while in the MONOSTABLE state, it is effective only if the IC is charging $C_X$. The voltage level of T2 then falls to $V_{ref}L$ level again.

Therefore the Q output stays high if the next trigger comes in before the time period set by $C_X$ and $R_X$.

If the 2nd trigger is very close to previous trigger, such as application during the discharge cycle, the 2nd trigger will not be effective.

The minimum time for effective 2nd trigger, $t_{rr}$ (min), depends on $V_{CC}$ and $C_X$.

(4) Reset operation

In normal operation, $\overline{CD}$ input is held high. If $\overline{CD}$ is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also, $Q_P$ turns on and $C_X$ is charged rapidly to $V_{CC}$.

This means if $\overline{CD}$ input is set low, the IC goes into a wait state.

## 13. Absolute Maximum Ratings (Note)

| Characteristics | Symbol | Note | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | -0.5 to 7.0 | V |
| Input voltage | $V_{IN}$ | | -0.5 to $V_{CC}$ + 0.5 | V |
| Output voltage | $V_{OUT}$ | | -0.5 to $V_{CC}$ + 0.5 | V |
| Input diode current | $I_{IK}$ | | ±20 | mA |
| Output diode current | $I_{OK}$ | | ±20 | mA |
| Output current | $I_{OUT}$ | | ±25 | mA |
| $V_{CC}$/ground current | $I_{CC}$ | | ±50 | mA |
| Power dissipation | $P_D$ | (Note 1) | 500 | mW |
| Storage temperature | $T_{stg}$ | | -65 to 150 | °C |

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: $P_D$ derates linearly with -8 mW/°C above 85°C.

## 14. Operating Ranges (Note)

| Characteristics | Symbol | Note | Test Condition | Rating | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | — | 2.0 to 6.0 | V |
| Input voltage | $V_{IN}$ | | — | 0 to $V_{CC}$ | V |
| Output voltage | $V_{OUT}$ | | — | 0 to $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | | — | -40 to 125 | °C |
| Input rise and fall times ($\overline{CD}$ only) | $t_r$,$t_f$ | | $V_{CC}$ = 4.5 V | 0 to 50 | μs |
| External capacitor | $C_X$ | (Note 1) | — | No limitation | F |
| External resistor | $R_X$ | (Note 1) | $V_{CC}$ = 2.0 V | ≥ 5 k | Ω |
| | | | $V_{CC}$ ≥ 3.0 V | ≥ 1 k | |

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either $V_{CC}$ or GND.

Note 1: The maximum allowable values of $C_X$ and $R_X$ are a function of leakage of capacitor $C_X$, the leakage of 74HC4538D, and leakage due to board layout and surface resistance.
Susceptibility to externally induced noise signals may occur for $R_X$ > 1 MΩ.

## 15. Electrical Characteristics

### 15.1. DC Characteristics (Unless otherwise specified, $T_a$ = 25 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | — | V |
| | | | | 4.5 | 3.15 | — | — | |
| | | | | 6.0 | 4.20 | — | — | V |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | — | 0.50 | V |
| | | | | 4.5 | — | — | 1.35 | |
| | | | | 6.0 | — | — | 1.80 | V |
| High-level output voltage (Q, $\overline{Q}$) | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 μA | 2.0 | 1.9 | 2.0 | — | V |
| | | | | 4.5 | 4.4 | 4.5 | — | |
| | | | | 6.0 | 5.9 | 6.0 | — | |
| | | | $I_{OH}$ = -4 mA | 4.5 | 4.18 | 4.31 | — | |
| | | | $I_{OH}$ = -5.2 mA | 6.0 | 5.68 | 5.80 | — | |
| Low-level output voltage (Q, $\overline{Q}$) | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2.0 | — | 0.0 | 0.1 | V |
| | | | | 4.5 | — | 0.0 | 0.1 | |
| | | | | 6.0 | — | 0.0 | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 | — | 0.17 | 0.26 | |
| | | | $I_{OL}$ = 5.2 mA | 6.0 | — | 0.18 | 0.26 | V |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | — | ±0.1 | μA |
| T2 terminal input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | — | ±0.5 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | — | 4.0 | μA |
| Active-state supply current (per circuit) | $I_{CC(opr)}$ | $V_{IN}$ = $V_{CC}$ or GND<br>T2 ext = 0.25 $V_{CC}$ | | 2.0 | — | 40 | 120 | μA |
| | | | | 4.5 | — | 250 | 350 | |
| | | | | 6.0 | — | 450 | 600 | |

## 15.2. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 85 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | V |
| | | | | 4.5 | 3.15 | — | |
| | | | | 6.0 | 4.20 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | 0.50 | V |
| | | | | 4.5 | — | 1.35 | |
| | | | | 6.0 | — | 1.80 | |
| High-level output voltage (Q, $\overline{Q}$) | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 μA | 2.0 | 1.9 | — | V |
| | | | | 4.5 | 4.4 | — | |
| | | | | 6.0 | 5.9 | — | |
| | | | $I_{OH}$ = -4 mA | 4.5 | 4.13 | — | |
| | | | $I_{OH}$ = -5.2 mA | 6.0 | 5.63 | — | |
| Low-level output voltage (Q, $\overline{Q}$) | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2.0 | — | 0.1 | V |
| | | | | 4.5 | — | 0.1 | |
| | | | | 6.0 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 | — | 0.33 | |
| | | | $I_{OL}$ = 5.2 mA | 6.0 | — | 0.33 | V |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | ±1.0 | μA |
| T2 terminal input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | ±5.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | 40.0 | μA |
| Active-state supply current (per circuit) | $I_{CC(opr)}$ | $V_{IN}$ = $V_{CC}$ or GND<br>T2 ext = 0.25 $V_{CC}$ | | 2.0 | — | 160 | μA |
| | | | | 4.5 | — | 400 | |
| | | | | 6.0 | — | 800 | |

## 15.3. DC Characteristics (Unless otherwise specified, $T_a$ = -40 to 125 °C)

| Characteristics | Symbol | Test Condition | | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | — | | 2.0 | 1.50 | — | V |
| | | | | 4.5 | 3.15 | — | |
| | | | | 6.0 | 4.20 | — | |
| Low-level input voltage | $V_{IL}$ | — | | 2.0 | — | 0.50 | V |
| | | | | 4.5 | — | 1.35 | |
| | | | | 6.0 | — | 1.80 | |
| High-level output voltage (Q, $\overline{Q}$) | $V_{OH}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = -20 μA | 2.0 | 1.9 | — | V |
| | | | | 4.5 | 4.4 | — | |
| | | | | 6.0 | 5.9 | — | |
| | | | $I_{OH}$ = -4 mA | 4.5 | 3.7 | — | |
| | | | $I_{OH}$ = -5.2 mA | 6.0 | 5.2 | — | |
| Low-level output voltage (Q, $\overline{Q}$) | $V_{OL}$ | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 20 μA | 2.0 | — | 0.1 | V |
| | | | | 4.5 | — | 0.1 | |
| | | | | 6.0 | — | 0.1 | |
| | | | $I_{OL}$ = 4 mA | 4.5 | — | 0.4 | |
| | | | $I_{OL}$ = 5.2 mA | 6.0 | — | 0.4 | |
| Input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | ±1.0 | μA |
| T2 terminal input leakage current | $I_{IN}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | ±10.0 | μA |
| Quiescent supply current | $I_{CC}$ | $V_{IN}$ = $V_{CC}$ or GND | | 6.0 | — | 80.0 | μA |
| Active-state supply current (per circuit) | $I_{CC(opr)}$ | $V_{IN}$ = $V_{CC}$ or GND<br>T2 ext = 0.25 $V_{CC}$ | | 2.0 | — | 160 | μA |
| | | | | 4.5 | — | 400 | |
| | | | | 6.0 | — | 800 | |

### 15.4. Timing Requirements (Unless otherwise specified, $T_a$ = 25 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Typ. | Limit | Unit |
|---|---|---|---|---|---|---|
| Minimum pulse width (A, $\overline{B}$) | $t_{w(L)}$,$t_{w(H)}$ | — | 2.0 | — | 75 | ns |
| | | | 4.5 | — | 15 | |
| | | | 6.0 | — | 13 | |
| Minimum pulse width ($\overline{CD}$) | $t_{w(L)}$ | — | 2.0 | — | 75 | ns |
| | | | 4.5 | — | 15 | |
| | | | 6.0 | — | 13 | |
| Minimum removal time | $t_{rem}$ | — | 2.0 | — | 25 | ns |
| | | | 4.5 | — | 5 | |
| | | | 6.0 | — | 4 | |
| Minimum retrigger time | $t_{rr}$ | $R_X$ = 1 kΩ, $C_X$ = 100 pF | 2.0 | 60 | — | ns |
| | | | 4.5 | 25 | — | |
| | | | 6.0 | 20 | — | |
| | | $R_X$ = 1 kΩ, $C_X$ = 0.01 μF | 2.0 | 1.8 | — | μs |
| | | | 4.5 | 0.8 | — | |
| | | | 6.0 | 0.7 | — | |

### 15.5. Timing Requirements (Unless otherwise specified, $T_a$ = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|---|
| Minimum pulse width (A, $\overline{B}$) | $t_{w(L)}$,$t_{w(H)}$ | — | 2.0 | 95 | ns |
| | | | 4.5 | 19 | |
| | | | 6.0 | 16 | |
| Minimum pulse width ($\overline{CD}$) | $t_{w(L)}$ | — | 2.0 | 95 | ns |
| | | | 4.5 | 19 | |
| | | | 6.0 | 16 | |
| Minimum removal time | $t_{rem}$ | — | 2.0 | 30 | ns |
| | | | 4.5 | 6 | |
| | | | 6.0 | 5 | |

### 15.6. Timing Requirements (Unless otherwise specified, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Limit | Unit |
|---|---|---|---|---|---|
| Minimum pulse width (A, $\overline{B}$) | $t_{w(L)}$,$t_{w(H)}$ | — | 2.0 | 110 | ns |
| | | | 4.5 | 22 | |
| | | | 6.0 | 19 | |
| Minimum pulse width ($\overline{CD}$) | $t_{w(L)}$ | — | 2.0 | 135 | ns |
| | | | 4.5 | 27 | |
| | | | 6.0 | 23 | |
| Minimum removal time | $t_{rem}$ | — | 2.0 | 40 | ns |
| | | | 4.5 | 8 | |
| | | | 6.0 | 7 | |

### 15.7. AC Characteristics (Unless otherwise specified, $C_L$ = 15 pF, $V_{CC}$ = 5 V, $T_a$ = 25 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Output transition time | $t_{TLH}$,$t_{THL}$ | — | — | 6 | 12 | ns |
| Propagation delay time (A, $\overline{B}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | — | — | 25 | 44 | |
| Propagation delay time ($\overline{CD}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | — | — | 25 | 44 | |

### 15.8. AC Characteristics (Unless otherwise specified, $C_L$ = 50 pF, $T_a$ = 25 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Note | Test Condition | $V_{CC}$ (V) | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Output transition time | $t_{TLH}$,$t_{THL}$ | | — | 2.0 | — | 30 | 75 | ns |
| | | | | 4.5 | — | 8 | 15 | |
| | | | | 6.0 | — | 7 | 13 | |
| Propagation delay time (A, $\overline{B}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | | — | 2.0 | — | 120 | 250 | ns |
| | | | | 4.5 | — | 30 | 50 | |
| | | | | 6.0 | — | 25 | 43 | |
| Propagation delay time ($\overline{CD}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | | — | 2.0 | — | 120 | 250 | ns |
| | | | | 4.5 | — | 30 | 50 | |
| | | | | 6.0 | — | 25 | 43 | |
| Output pulse width | $t_{wOUT}$ | | $C_X$ = 0 F<br>$R_X$ = 5 kΩ ($V_{CC}$ = 2.0V)<br>$R_X$ = 1 kΩ ($V_{CC}$ = 4.5 V, 6.0 V) | 2.0 | — | 540 | 1200 | ns |
| | | | | 4.5 | — | 180 | 250 | |
| | | | | 6.0 | — | 150 | 200 | |
| | | | $C_X$ = 0.01 μF<br>$R_X$ = 10 kΩ | 2.0 | 70 | 83 | 96 | μs |
| | | | | 4.5 | 69 | 77 | 85 | |
| | | | | 6.0 | 69 | 77 | 85 | |
| | | | $C_X$ = 0.1 μF<br>$R_X$ = 10 kΩ | 2.0 | 0.73 | 0.79 | 0.85 | ms |
| | | | | 4.5 | 0.71 | 0.75 | 0.79 | |
| | | | | 6.0 | 0.71 | 0.75 | 0.79 | |
| Output pulse width error between circuits (in same package) | $\Delta t_{wOUT}$ | | — | | — | ±1 | — | % |
| Input capacitance | $C_{IN}$ | | — | | — | 5 | 10 | pF |
| Power dissipation capacitance | $C_{PD}$ | (Note 1) | — | | — | 40 | — | pF |

Note 1: $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC'} \times Duty/100 + I_{CC}/2$ (per circuit),

($I_{CC'}$: Active supply current),

(Duty: %)

### 15.9. AC Characteristics (Unless otherwise specified, $C_L$ = 50 pF, $T_a$ = -40 to 85 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Output transition time | $t_{TLH}$,$t_{THL}$ | — | 2.0 | — | 95 | ns |
| | | | 4.5 | — | 19 | |
| | | | 6.0 | — | 16 | |
| Propagation delay time (A, $\overline{B}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | — | 2.0 | — | 315 | ns |
| | | | 4.5 | — | 63 | |
| | | | 6.0 | — | 54 | |
| Propagation delay time ($\overline{CD}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | — | 2.0 | — | 315 | ns |
| | | | 4.5 | — | 63 | |
| | | | 6.0 | — | 54 | |
| Output pulse width | $t_{wOUT}$ | $C_X$ = 0 F<br>$R_X$ = 5 kΩ ($V_{CC}$ = 2.0V)<br>$R_X$ = 1 kΩ ($V_{CC}$ = 4.5 V, 6.0 V) | 2.0 | — | 1500 | ns |
| | | | 4.5 | — | 320 | ns |
| | | | 6.0 | — | 260 | ns |
| | | $C_X$ = 0.01 μF<br>$R_X$ = 10 kΩ | 2.0 | 70 | 96 | μs |
| | | | 4.5 | 69 | 85 | μs |
| | | | 6.0 | 69 | 85 | μs |
| | | $C_X$ = 0.1 μF<br>$R_X$ = 10 kΩ | 2.0 | 0.71 | 0.86 | ms |
| | | | 4.5 | 0.70 | 0.80 | ms |
| | | | 6.0 | 0.70 | 0.80 | ms |
| Input capacitance | $C_{IN}$ | — | | — | 10 | pF |

### 15.10. AC Characteristics (Unless otherwise specified, $C_L$ = 50 pF, $T_a$ = -40 to 125 °C, Input: $t_r = t_f$ = 6 ns)

| Characteristics | Symbol | Test Condition | $V_{CC}$ (V) | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Output transition time | $t_{TLH}$,$t_{THL}$ | — | 2.0 | — | 110 | ns |
| | | | 4.5 | — | 22 | |
| | | | 6.0 | — | 19 | |
| Propagation delay time (A, $\overline{B}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | — | 2.0 | — | 380 | ns |
| | | | 4.5 | — | 76 | |
| | | | 6.0 | — | 65 | |
| Propagation delay time ($\overline{CD}$ - Q, $\overline{Q}$) | $t_{PLH}$,$t_{PHL}$ | — | 2.0 | — | 380 | ns |
| | | | 4.5 | — | 76 | |
| | | | 6.0 | — | 65 | |
| Output pulse width | $t_{wOUT}$ | $C_X$ = 0 F<br>$R_X$ = 5 kΩ ($V_{CC}$ = 2.0V)<br>$R_X$ = 1 kΩ ($V_{CC}$ = 4.5 V, 6.0 V) | 2.0 | — | 1500 | ns |
| | | | 4.5 | — | 320 | |
| | | | 6.0 | — | 260 | |
| | | $C_X$ = 0.01 μF<br>$R_X$ = 10 kΩ | 2.0 | 70 | 96 | μs |
| | | | 4.5 | 69 | 85 | |
| | | | 6.0 | 69 | 85 | |
| | | $C_X$ = 0.1 μF<br>$R_X$ = 10 kΩ | 2.0 | 0.71 | 0.87 | ms |
| | | | 4.5 | 0.70 | 0.81 | |
| | | | 6.0 | 0.70 | 0.81 | |

## 16. Characteristics Curves (Note)

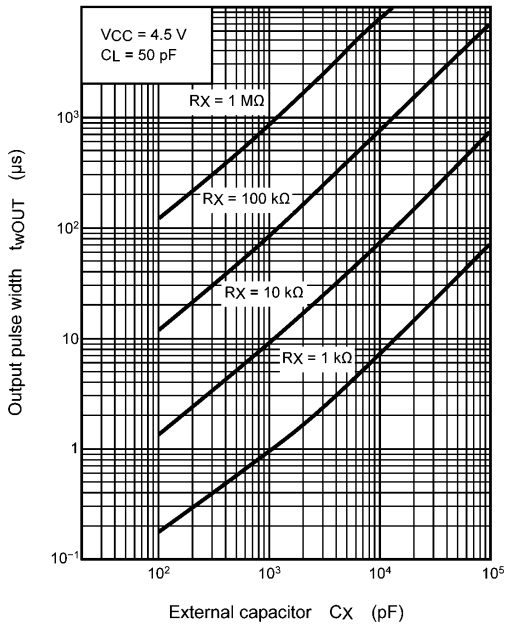



Fig. 16.1 $t_{WOUT}$ - $C_X$ (typ.)

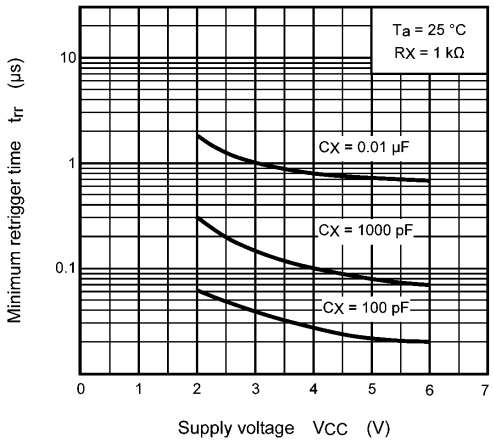



Fig. 16.2 $t_{rr}$ - $V_{CC}$ (typ.)

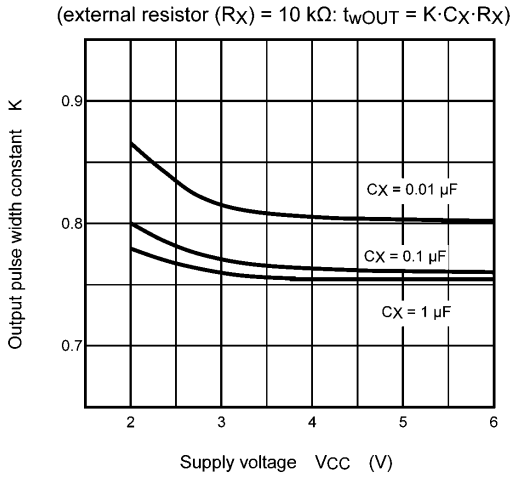
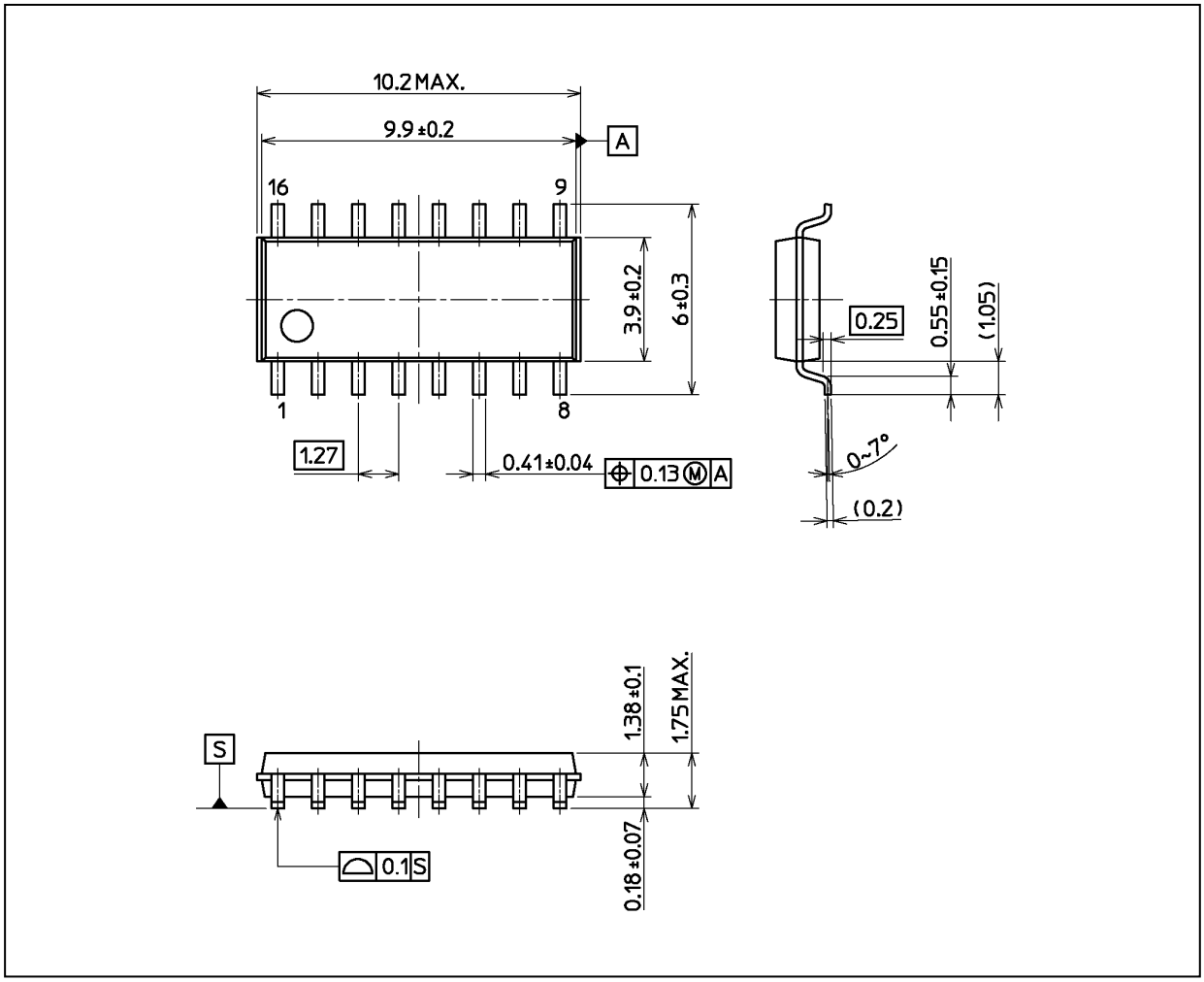



Fig. 16.3 Output Pulse Width Constant K - Supply Voltage (typ.)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm




Weight: 0.15 g (typ.)

| Package Name(s) |
| --- |
| Nickname: SOIC16 |

## RESTRICTIONS ON PRODUCT USE

- Toshiba Corporation, and its subsidiaries and affiliates (collectively "TOSHIBA"), reserve the right to make changes to the information in this document, and related hardware, software and systems (collectively "Product") without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**