TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74HCT373AP,TC74HCT373AF

Octal D-Type Latch with 3-State Output

The TC74HCT373A is a high speed CMOS OCTAL LATCH with 3-STATE OUTPUT fabricated with silicon gate C^2MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

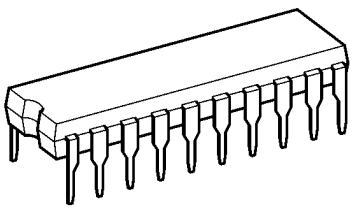
Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

These 8-bit D-type latches are controlled by a latch enable input (LE) and an output enable input ($\overline{OE}$).

When the $\overline{OE}$ input is high, the eight outputs are in a high impedance state.

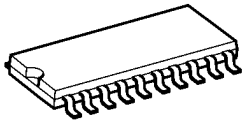
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

TC74HCT373AP



DIP20-P-300-2.54A

TC74HCT373AF



SOP20-P-300-1.27A

Weight

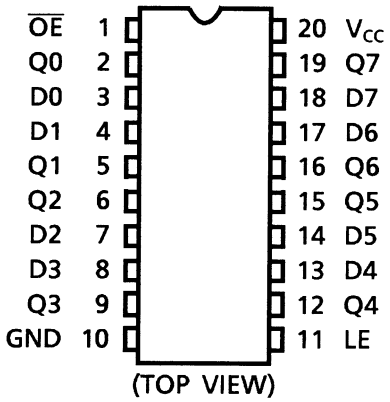
DIP20-P-300-2.54A : 1.30 g (typ.)

SOP20-P-300-1.27A : 0.22 g (typ.)

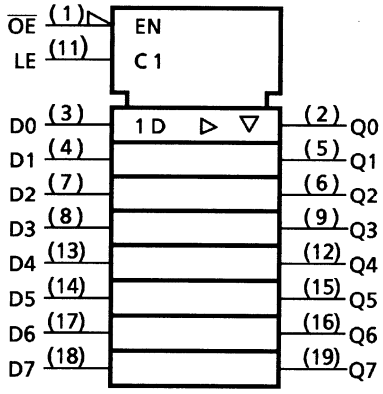
Features

- High speed: t_{pd} = 17 ns (typ.) at V_{CC} = 5 V
- Low power dissipation: I_{CC} = 4 μA (max) at Ta = 25°C
- Compatible with TTL outputs: V_{IH} = 2 V (min)
  V_{IL} = 0.8 V (max)
- Wide interfacing ability: LSTTL, NMOS, CMOS
- Output drive capability: 15 LSTTL loads
- Symmetrical output impedance: $|I_{OH}| = I_{OL}$ = 6 mA (min)
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Pin and function compatible with 74LS373

Pin Assignment



IEC Logic Symbol



Truth Table

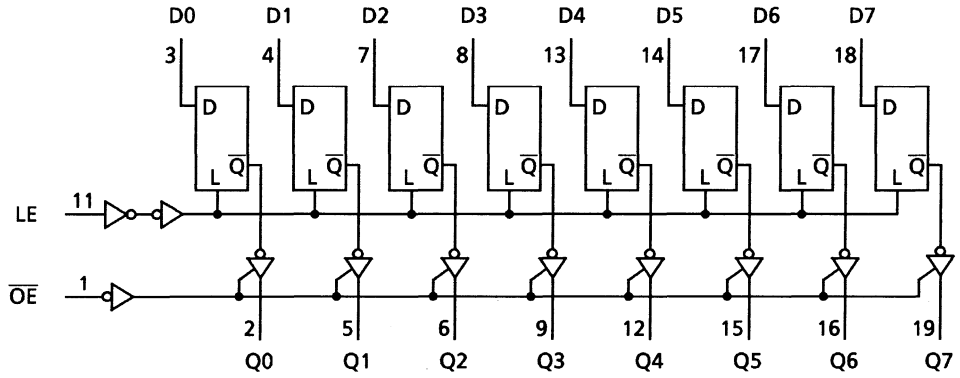
Inputs			Output
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	Q_n
L	H	L	L
L	H	H	H

X: Don't care

Z: High impedance

Q_n: Q outputs are latched at the time when the LE input is taken to a low logic level.

System Diagram



Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5~7	V
DC input voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC output voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	±20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±35	mA
DC V_{CC}/ground current	I_{CC}	±75	mA
Power dissipation	P_D	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	T_{stg}	−65~150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40~65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C shall be applied until 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	4.5~5.5	V
Input voltage	V_{IN}	0~V_{CC}	V
Output voltage	V_{OUT}	0~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	t_r, t_f	0~500	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40~85°C Min	Ta = −40~85°C Max	Unit
High-level input voltage	V_{IH}	—		4.5~5.5	2.0	—	—	2.0	—	V
Low-level input voltage	V_{IL}	—		4.5~5.5	—	—	0.8	—	0.8	V
High-level output voltage	V_{OH}	V_{IN} = V_{IH}	I_{OH} = −20 μA	4.5	4.4	4.5	—	4.4	—	V
			I_{OH} = −6 mA	4.5	4.18	4.31	—	4.13	—	
Low-level output voltage	V_{OL}	V_{IN} = V_{IL}	I_{OL} = 20 μA	4.5	—	0.0	0.1	—	0.1	V
			I_{OL} = 6 mA	4.5	—	0.17	0.26	—	0.33	
3-state output off-state current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		5.5	—	—	±0.5	—	±5.0	μA
Input leakage current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	μA
	I_C	Per input: V_{IN} = 0.5 V or 2.4 V Other input: V_{CC} or GND		5.5	—	—	2.0	—	2.9	mA

Timing Requirements (input: $t_r = t_f = 6$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Ta = 25°C Typ.	Ta = 25°C Limit	Ta = −40~85°C Limit	Unit
Minimum pulse width (LE)	$t_{W(H)}$	—	4.5	—	15	19	ns
			5.5	—	14	17	
Minimum set-up time (Dn)	t_s	—	4.5	—	10	13	ns
			5.5	—	9	12	
Minimum hold time (Dn)	t_h	—	4.5	—	5	5	ns
			5.5	—	5	5	

AC Characteristics (C_L = 50 pF, input: $t_r = t_f$ = 6 ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40~85°C		Unit
			CL (pF)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Output transition time	t_{TLH} t_{THL}	—	50	4.5	—	7	12	—	15	ns
				5.5	—	6	11	—	14	
Propagation delay time (LE-Q)	t_{pLH} t_{pHL}	—	50	4.5	—	19	30	—	38	ns
				5.5	—	16	27	—	34	
			150	4.5	—	24	38	—	48	
				5.5	—	22	34	—	43	
Propagation delay time (D-Q)	t_{pLH} t_{pHL}	—	50	4.5	—	20	30	—	38	ns
				5.5	—	18	27	—	34	
			150	4.5	—	25	38	—	48	
				5.5	—	22	34	—	43	
Output enable time	t_{pZL} t_{pZH}	R_L = 1 kΩ	50	4.5	—	19	30	—	38	ns
				5.5	—	16	27	—	34	
			150	4.5	—	24	38	—	48	
				5.5	—	22	34	—	43	
Output disable time	t_{pLZ} t_{pHZ}	R_L = 1 kΩ	50	4.5	—	20	30	—	38	ns
				5.5	—	18	27	—	34	
Input capacitance	C_{IN}	—			—	5	10	—	10	pF
Output capacitance	C_{OUT}	—			—	10	—	—	—	pF
Power dissipation capacitance	C_{PD} (Note)	—			—	36	—	—	—	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

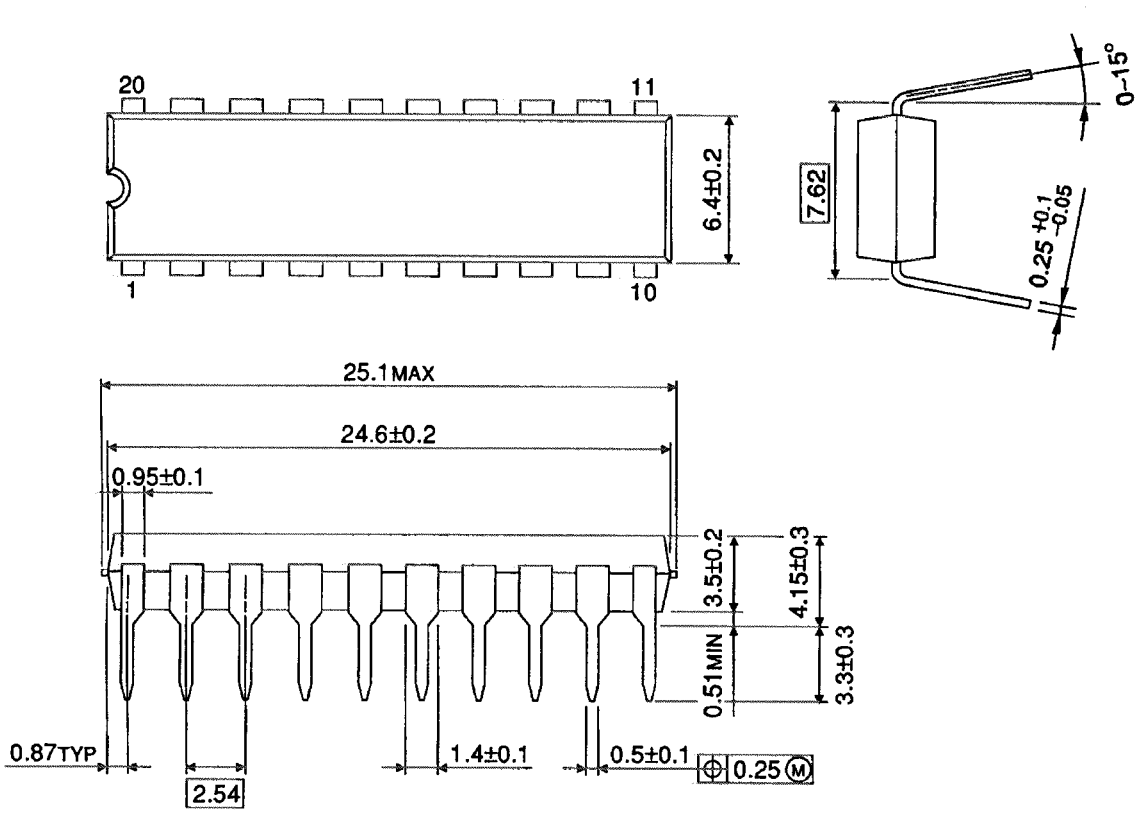
I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per latch)

And the total C_{PD} when n pcs. of flip flop operate can be gained by the following equation:

C_{PD} (total) = 19 + 17·n

Package Dimensions

DIP20-P-300-2.54A Unit : mm



Weight: 1.30 g (typ.)

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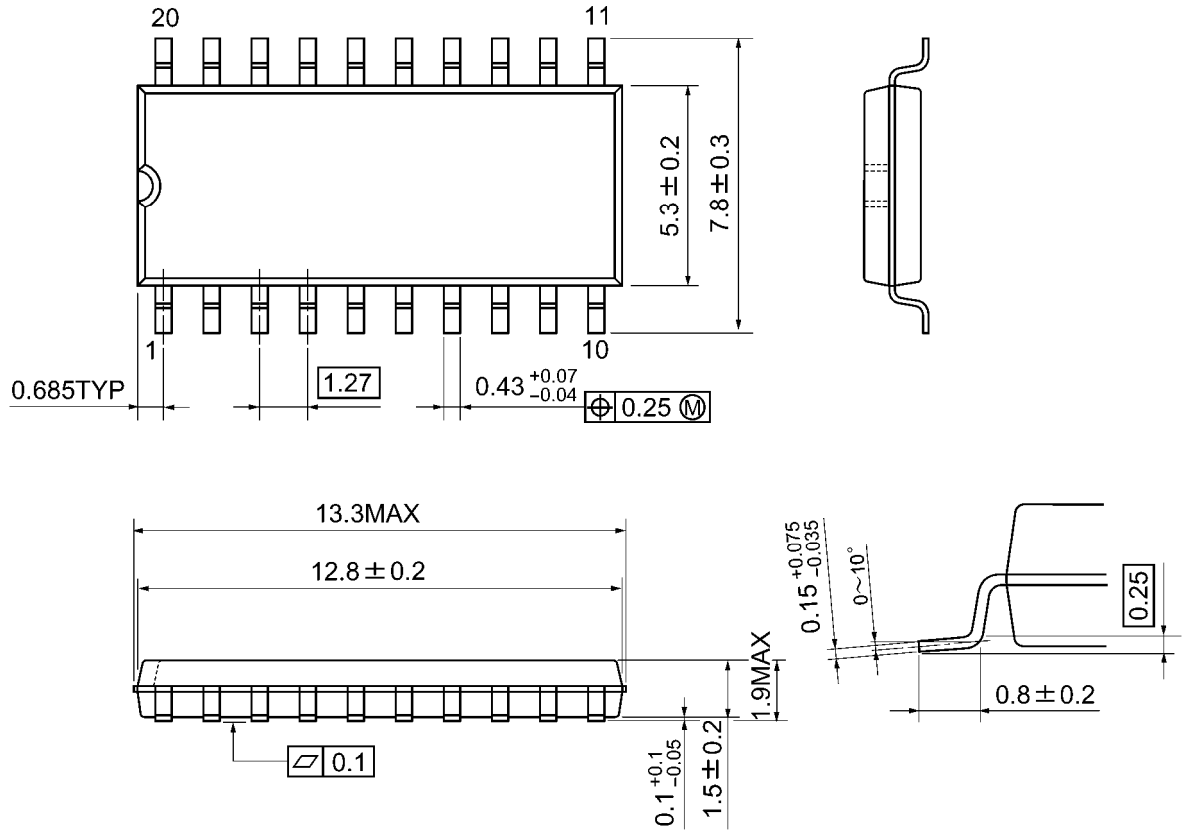

Weight: 0.22 g (typ.)

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