

CMOS 8-BIT MICROCONTROLLERS

TMP90C041AN/TMP90C041AF

1. OUTLINE AND CHARACTERISTICS

The TMP90C041A is a high-speed advanced 8-bit micro controller applicable to a variety of equipment.

With its 8-bit CPU, A/D converter, multi-function timer/event counter and general-purpose serial interface integrated into a single CMOS chip, the TMP90C041A allows the expansion of external memories for programs (up to 64K byte) and data (1M byte).

The TMP90C041AN is a 64-pin shrink DIP product. (SDIP64-P-750)

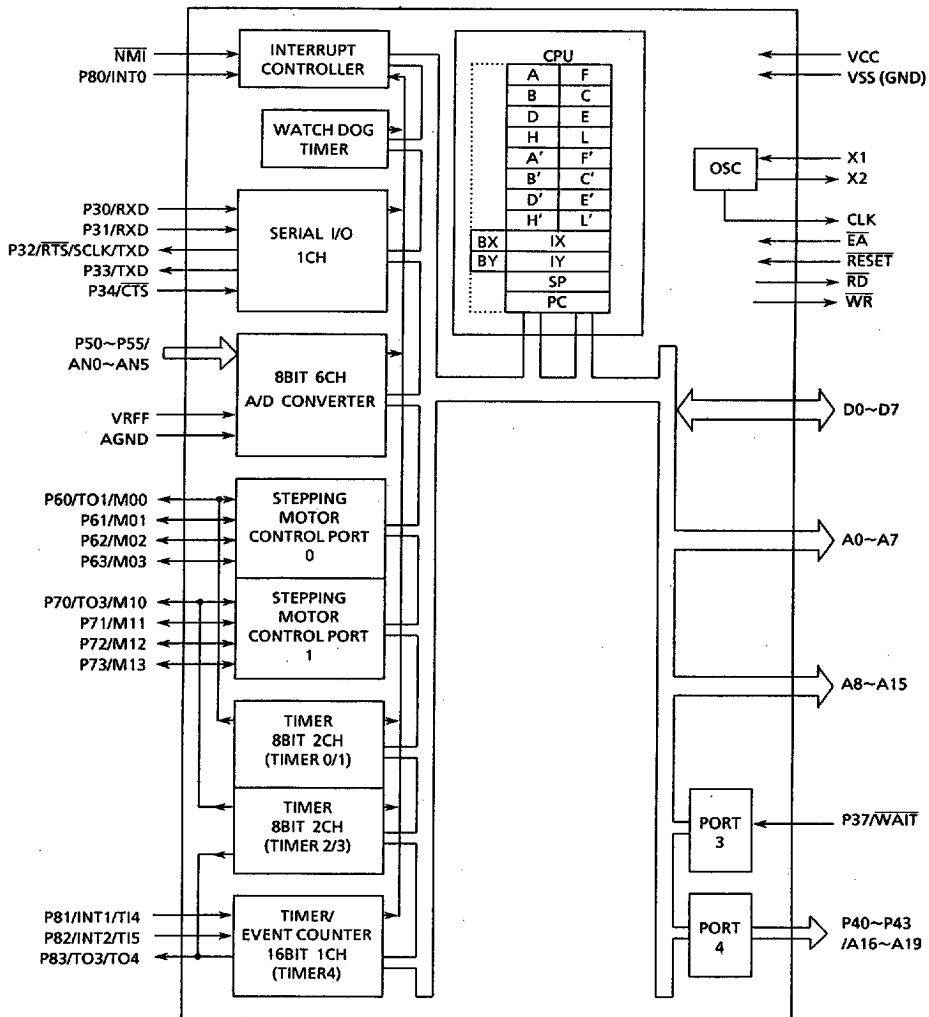
The TMP90C041AF is a 64-pin flat package product. (QFP64-P-1420A)

The characteristics of the TMP90C041A include:

- (1) Powerful instructions
163 basic instructions, including
Multiplication, division, 16-bit arithmetic operations, bit manipulation instructions
- (2) Minimum instruction executing time: 250 ns (at 16 MHz oscillation frequency)
- (3) Memory expansion
External program memory: 64K byte
External data memory: 1M byte
- (4) 8-bit A/D converter (6 channels)
- (5) General-purpose serial interface (1 channel)
Asynchronous mode, I/O interface mode
- (6) Multi-function 16-bit timer/event counter (1 channel)
- (7) 8-bit timers (4 channels)
- (8) Stepping motor control port (2 channels)
- (9) Input/Output ports (28 pins)
- (10) Interrupt function: 10 internal interrupts and 4 external interrupts
- (11) Micro Direct Memory Access (μ DMA) function (11 channels)
- (12) Watchdog timer
- (13) Standby function (4 HALT modes)

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Figure 1 TMP90C041A Block Diagram

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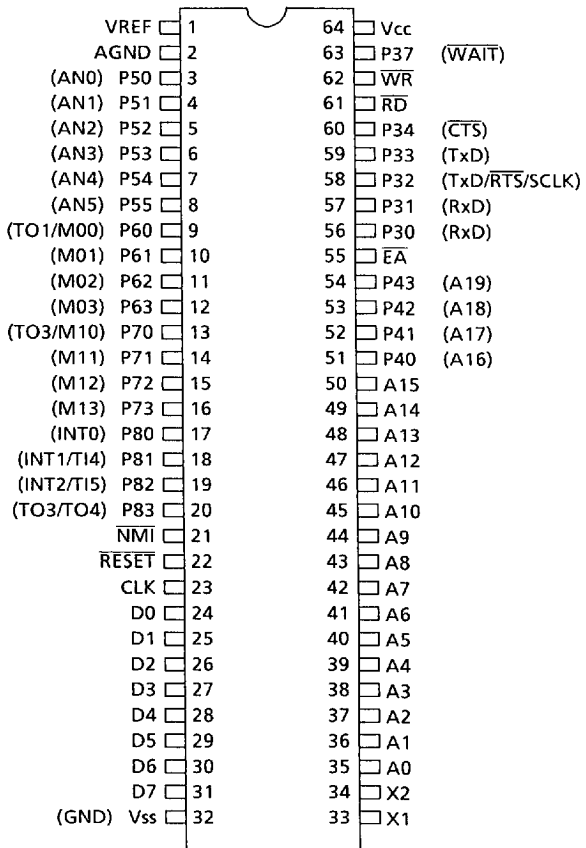
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2. PIN ASSIGNMENT AND FUNCTIONS

The assignment of input/output pins, their names and functions are described below.

2.1 Pin Assignment

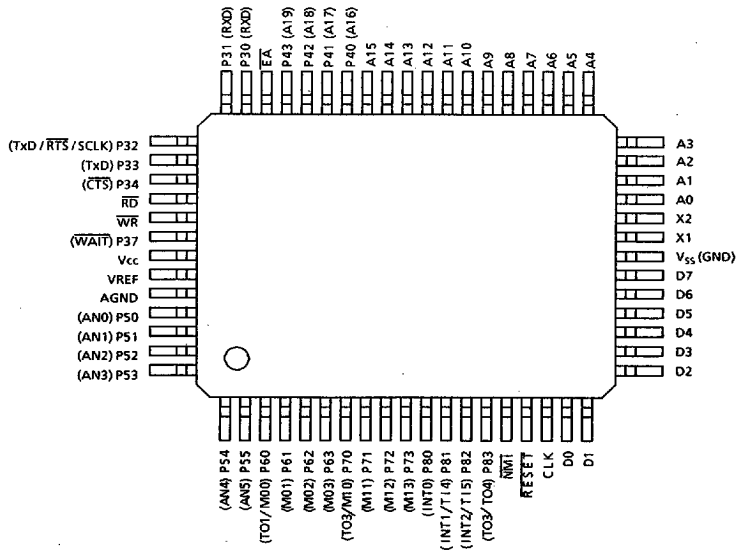
Figure 2.1-(1) shows pin assignment of the TMP90C041AN.



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Figure 2.1- (1) Pin Assignment (Shrink Dual Inline Package)

Figure 2.1- (2) shows pin assignment of the TMP90C041AF.



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Figure 2.1- (2) Pin Assignment (Flat Package)

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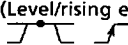
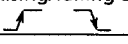
2.2 Pin Names and Functions

The names of input/output pins and their functions are summarized in Table 2.2.

Table 2.2 Pin Names and Functions (1/2)

Pin Name	No. of pins	I/O 3 states	Function
D0~D7	8	3 states	Data bus: Also functions as 8-bit bidirectional data bus for external memory
A0~A7	8	Output	Address bus: The lower 8 bits address bus for external memory
A8~A15	8	Output	Address bus: The upper 8 bits address bus for external memory
P30 /RxD	1	Input	Port 30: 1-bit input port Receiver Serial Data
P31 /RxD	1	Input	Port 31: 1-bit input port Receiver Serial Data
P32 /TxD /RTS /SCLK	1	Output	Port 32: 1-bit output port Transmitter serial Data Request to send serial data Serial clock output
P33 /TxD	1	Output	Port 33: 1-bit output port Transmitter Serial Data
P34 /CTS	1	Input	Port 34: 1-bit input port Clear to send Serial data
RD	1	Output	Read: Generates strobe signal for reading external memory
WR	1	Output	Write: Generates strobe signal for writing into external memory
P37 /WAIT	1	Input	Port 37: 1-bit input port Wait: Input pin for connecting slow speed memory or peripheral LSI
P40~P43 /A16~A19	4	Output	Port 4: 4-bit output port that allows selection of Port/Address Bus on bit basis Address bus: Also functions as address bus for external memory (4 bits of bank address)
P50~P55 /AN0~AN5	6	Input	Port 5: 6-bit input port Analog input: 6 analog inputs to A/D converter
VREF	1		Input of reference voltage to A/D converter

Table 2.2 Pin Names and Functions (2/2)

Pin Name	No. of pins	I/O 3 states	Function
AGND	1		Ground pin for A/D converter
P60~P63 /M00~M03 /TO1	4	I/O	Port 6: 4-bit I/O port that allows I/O selection on bit basis
		Output	Stepping motor control port 0
		Output	Timer output 1: Output of Timer 0 or 1
P70~P73 /M10~M13 /TO3	4	I/O	Port 7: 4-bit I/O port that allows I/O selection on bit basis
		Output	Stepping motor control port 1
		Output	Timer output 3: Output of Timer 2 or 3
P80 /INT0	1	Input	Port 80: 1-bit input port
			Interrupt request pin 0: interrupt request pin (Level/rising edge is programmable) 
P81 /INT1 /TI4	1	Input	Port 81: 1-bit input port
			Interrupt request pin 1: interrupt request pin (Rising/falling edge is programmable) 
			Timer input 4: Counter/capture trigger signal for Timer 4
P82 /INT2 /TI5	1	Input	Port 82: 1-bit input port
			Interrupt request pin 2: rising edge interrupt request pin
			Timer input 5: capture trigger signal for Timer 4
P83 /TO3 /TO4	1	Output	Port 83: 1-bit output port
			Timer output 3/4: Output of Timer 2, 3 or 4
NMI	1	Input	Non-maskable interrupt request pin: Falling edge interrupt request pin 
CLK	1	Output	Clock output: Generates clock pulse at 1/4 frequency of clock oscillation. It is Pulled up internally during resetting.
EA	1	Input	External access: Connects with GND pin in the TMP90C041A with no internal ROM.
RESET	1	Input	Reset : Initializes the TMP90C041A. (Built-in pull-up resister)
X1/X2	2	Input/ Output	Pins for quartz crystal or ceramic resonator
Vcc	1		Power supply (+ 5V)
Vss (GND)	1		Ground (0V)

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3. OPERATION

The following explains the TMP90C041A functions and basic operations.

The CPU functions and internal I/O functions of the TMP90C041A are the same as the TMP90C840A.

Refer to the “TMP90C840A” section concerning functions which are not explained the following.

3.1 CPU

The TMP90C041A has a internal high-performance 8-bit CPU.

Refer to the “TLCS-90 CPU” section concerning CPU operation.

3.2 Memory Map

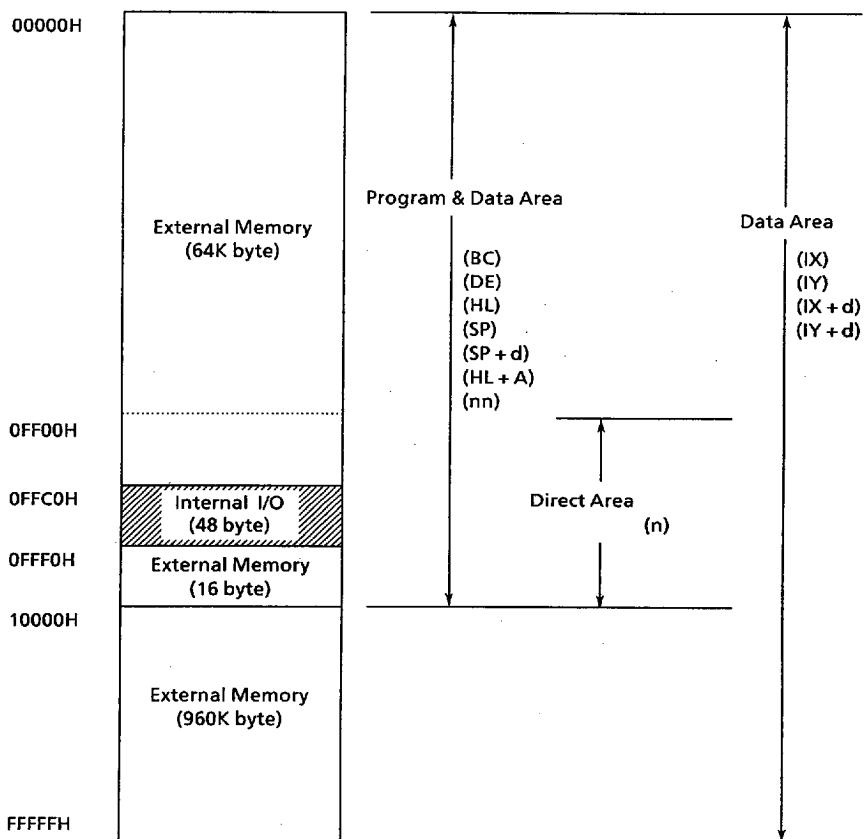
The TMP90C041A supports a program memory of up to 64K bytes and a data memory of maximum 1M bytes.

The program memory may be assigned to the address space from 00000H to 0FFFFH, while the data memory can be allocated to any address from 00000H to FFFFFH.

(1) Internal I/O

The TMP90C041A provides a 48-byte address space as an internal I/O area, whose addresses range from FFC0H to FFEFH. This I/O area can be accessed by the CPU using a short opcode in the “direct addressing mode”.

Figure 3.1 is a memory map indicating the areas accessible by the CPU in the respective addressing mode.



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Figure 3.1 Memory Map

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4. ELECTRICAL CHARACTERISTICS

TMP90C041AN/TMP90C041AF

4.1 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	- 0.5 ~ + 6.5	V
V_{IN}	Input voltage	- 0.5 ~ $V_{CC} + 0.5$	V
P_D	Power dissipation ($T_a = 70^\circ\text{C}$)	F 500 N 600	mW
T_{SOLDER}	Soldering temperature (10 s)	260	$^\circ\text{C}$
T_{STG}	Storage temperature	- 65 ~ 150	$^\circ\text{C}$
T_{OPR}	Operating temperature	- 20 ~ 70	$^\circ\text{C}$

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4.2 DC Characteristics

$T_A = -20 \sim 70^\circ\text{C}$ $V_{CC} = 5V \pm 10\%$
 Typical Values are for $T_A = 25^\circ\text{C}$ and $V_{CC} = 5V$.

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (D0~D7)	- 0.3	0.8	V	
V_{IL1}	P3, P5, P6, P7, P8	- 0.3	0.3 V_{CC}	V	
V_{IL2}	RESET, INT0, NMI	- 0.3	0.25 V_{CC}	V	
V_{IL3}	X1	- 0.3	0.2 V_{CC}	V	
V_{IH}	Input High Voltage (D0~D7)	2.2	$V_{CC} + 0.3$	V	
V_{IH1}	P3, P5, P6, P7, P8	0.7 V_{CC}	$V_{CC} + 0.3$	V	
V_{IH2}	RESET, INT0, NMI	0.75 V_{CC}	$V_{CC} + 0.3$	V	
V_{IH3}	X1	0.8 V_{CC}	$V_{CC} + 0.3$	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 1.6\text{mA}$
V_{OH} V_{OH1} V_{OH2}	Output High Voltage	2.4 0.75 V_{CC} 0.9 V_{CC}		V V V	$I_{OH} = -400\mu\text{A}$ $I_{OH} = -100\mu\text{A}$ $I_{OH} = -20\mu\text{A}$
I_{DAR}	Darlington Drive Current (8 I/O pins)	- 1.0	- 3.5	mA	$V_{EXT} = 1.5V$ $R_{EXT} = 1.1\text{k}\Omega$
I_{LI}	Input Leakage Current	0.02 (Typ)	± 5	μA	$0.0 \leq V_{in} \leq V_{CC}$
I_{LO}	Output Leakage Current	0.05 (Typ)	± 10	μA	$0.2 \leq V_{in} \leq V_{CC} - 0.2$
I_{CC}	Operating Current (RUN) Idle 1 Idle 2	19 (Typ) 1.6 (Typ) 9 (Typ)	30 6 15	mA mA mA	$t_{OSC} = 16\text{MHz}$
	STOP ($T_A = -20 \sim 70^\circ\text{C}$) STOP ($T_A = 0 \sim 50^\circ\text{C}$)	0.2 (Typ)	50 10	μA μA	$0.2 \leq V_{in} \leq V_{CC} - 0.2$
R RST	RESET Pull Up Resistor	50	150	$\text{k}\Omega$	
CIO	Pin Capacitance		10	pF	testfreq = 1MHz
V_{TH}	Schmitt width RESET, NMI, INT0	0.4	1.0 (Typ)	V	

Note : I_{DAR} is guaranteed for a total of up to 8 optional ports.

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4.3 AC Characteristics

TA = -20~70°C Vcc = 5V ± 10%
CL = 50pF

Symbol	Parameter	Variable		10MHz Clock		16MHz Clock		Unit
		Min	Max	Min	Max	Min	Max	
tOSC	OSC. Period = x	62.5	1000	100		62.5		ns
tCYC	CLK Period	4x	4x	400		250		ns
tWL	CLK Low width	2x - 40		160		85		ns
tWH	CLK High width	2x - 40		160		85		ns
tAC	Address Setup to $\overline{RD}$, $\overline{WR}$	x - 45		55		17		ns
tRR	$\overline{RD}$ Low width	2.5x - 40		210		115		ns
tCA	Address Hold Time After $\overline{RD}$, $\overline{WR}$	0.5x - 26		24		5		ns
tAD	Address to Valid Data In		3.5x - 95		255		124	ns
tRD	$\overline{RD}$ to Valid Data In		2.5x - 80		170		77	ns
tHR	Input Data Hold After $\overline{RD}$	0		0		0		ns
tWW	$\overline{WR}$ Low width	2.5x - 40		210		115		ns
tDW	Data Setup to $\overline{WR}$	2x - 50		150		75		ns
tWD	Data Hold After $\overline{WR}$	20	70	20	70	20	70	ns
tCWA	$\overline{RD}$, $\overline{WR}$ to Valid WAIT		1.5x - 80		70		14	ns
tAWA	Address to Valid WAIT		2.5x - 130		120		27	ns
tWAS	WAIT Setup to CLK	50		50		50		ns
tWAH	WAIT Hold After CLK	0		0		0		ns
tRV	$\overline{RD}$ / $\overline{WR}$ Recovery Time	1.5x - 35		115		58		ns
tCPW	CLK to Port Data Output		x + 200		300		263	ns
tPRC	Port Data Setup to CLK	200		200		200		ns
tCPR	Port Data Hold After CLK	100		100		100		ns
tCHCL	$\overline{RD}$ / $\overline{WR}$ Hold After CLK	x - 52		48		10		ns
tCLC	$\overline{RD}$ / $\overline{WR}$ Setup to CLK	1.5x - 25		125		68		ns
tCLHA	Address Hold After CLK	1.5x - 80		70		13		ns
tACL	Address Setup to CLK	2.5x - 80		170		76		ns
tCLD	Data Setup to CLK	x - 50		50		12		ns

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- AC output level High 2.2V/Low 0.8V
- AC input level High 2.4V/Low 0.45V (D0 - D7)
High 0.8Vcc/Low 0.2Vcc (excluding D0 - D7)

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4.4 A/D Conversion Characteristics

TA = -20~70°C Vcc = 5V ± 10%

Symbol	Parameter	Min	Typ	Max	Unit
VREF	Analog reference voltage	Vcc - 1.5	Vcc	Vcc	V
AGND	Analog reference voltage	Vss	Vss	Vss	
VAIN	Allowable analog input voltage	Vss		Vcc	
IREF	Supply current for analog reference voltage		0.5	1.0	mA
Error 1MHz < fc < 12.5MHz	Total error (TA = 25°C, Vcc = Vref = 5.0V)		1.0		LSB
	Total error			2.5	
Error 12.5 < fc < 16MHz	Total error (TA = 25°C, Vcc = Vref = 5.0V)		2.0		LSB
	Total error			3.5	

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4.5 Zero- Cross Characteristics

TA = -20~70°C Vcc = 5V ± 10%

Symbol	Parameter	Condition	Min	Max	Unit
Vzx	Zero- cross detection input	AC coupling C = 0.1μF	1	1.8	VAC p - p
Azx	Zero- cross accuracy	50/60Hz sine wave		135	mV
Fzx	Zero- cross detection input frequency		0.04	1	kHz

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4.6 Serial Channel Timing – I/O Interface Mode

TA = -20~70°C Vcc = 5V ± 10%
CL = 50pF

Symbol	Parameter	Variable		10MHz Clock		16MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
tscy	Serial Port Clock Cycle Time	8x		800		500		ns
toss	Output Data Setup SCLK Rising Edge	6x - 150		450		225		ns
tohs	Output Data Hold After SCLK Rising Edge	2x - 80		120		45		ns
tHSR	Input Data Hold After SCLK Rising Edge	0		0		0		ns
tSRD	SCLK Rising Edge to Input DATA Valid		6x - 150		450		225	ns

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4.7 16-Bit Event Counter

TA = -20~70°C Vcc = 5V ± 10%

Symbol	Parameter	Variable		10MHz Clock		16MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
tvCK	TI4 clock cycle	8x + 100		900		600		ns
tvCKL	TI4 Low clock pulse width	4x + 40		440		290		ns
tvCKH	TI4 High clock pulse width	4x + 40		440		290		ns

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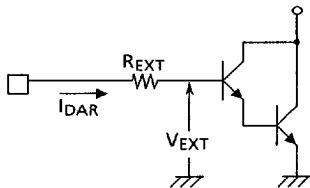
4.8 Interrupt Operation

TA = -20~70°C Vcc = 5V ± 10%

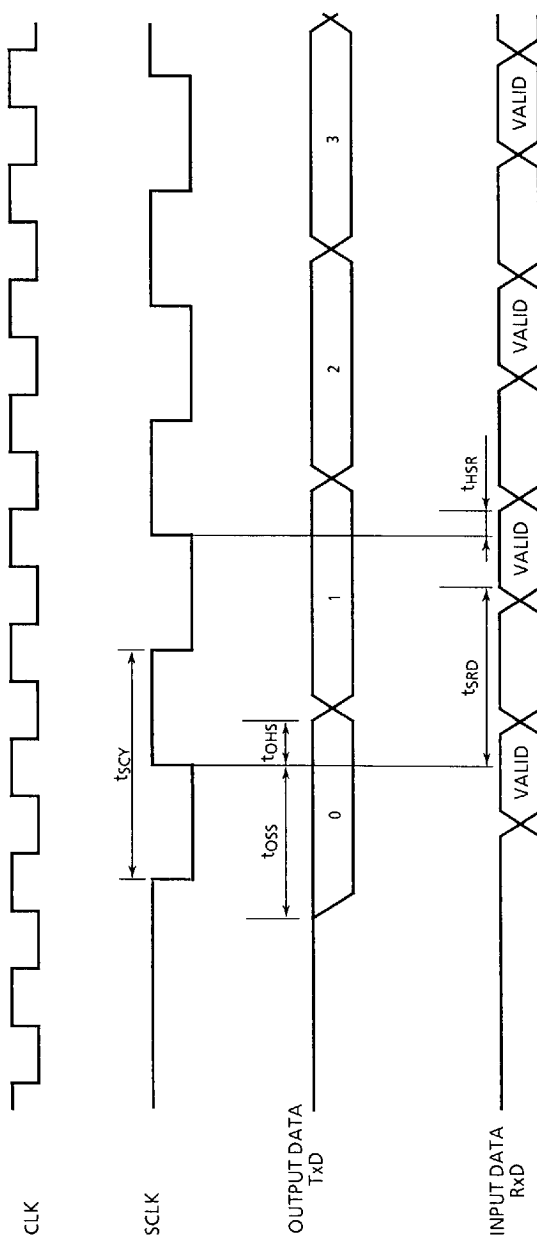
Symbol	Parameter	Variable		10MHz Clock		16MHz Clock		Units
		Min	Max	Min	Max	Min	Max	
tINTAL	NMI, INT0 Effective pulse width ()	4x		400		250		ns
tINTAH	NMI, INT0 Effective pulse width ()	4x		400		250		ns
tINTBL	INT1, INT2 Effective pulse width ()	8x + 100		900		600		ns
tINTBH	INT1, INT2 Effective pulse width ()	8x + 100		900		600		ns

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(Reference) Definition of IDAR



4.9 I/O Interface Mode Timing Chart

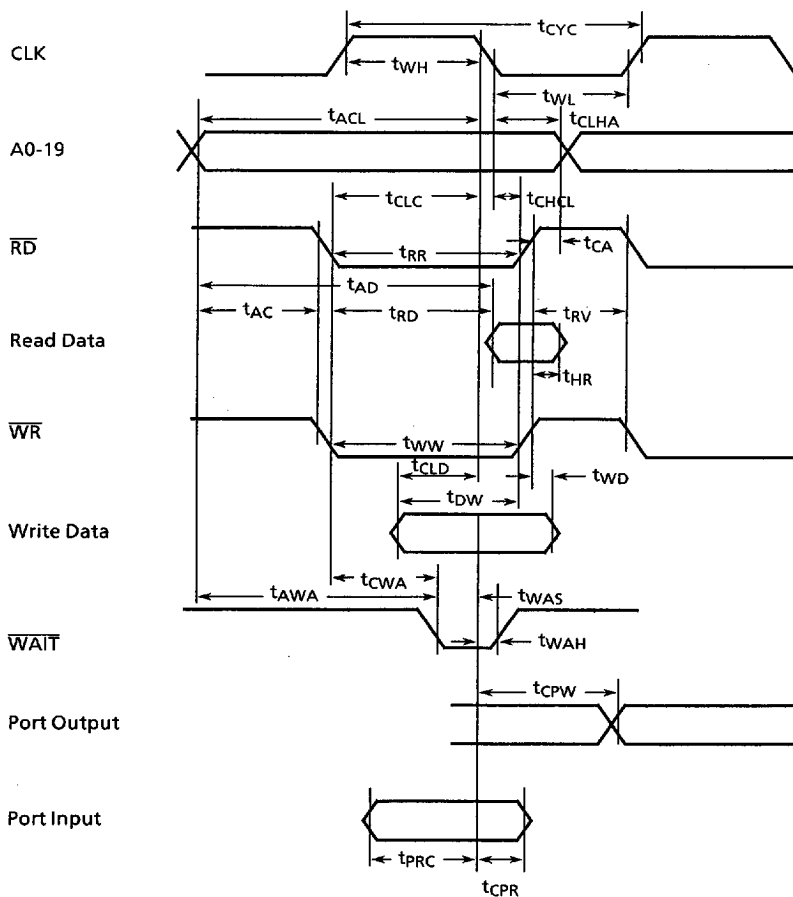


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4.10 Timing Chart



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5. DIFFERENT POINTS BETWEEN TMP90C841A AND TMP90C041A

Specifications of TMP90C841A and TMP90C041A are the same except below.

TMP90C841A system, not using internal RAM and internal I/O functions as shown below, can be substituted by TMP90C041A system. To substitute the TMP90C841A system using the internal RAM by the TMP90C041A system, it is necessary to attach the external RAM to the address corresponded to the internal address.

Name	TMP90C841A	TMP90C041A
RAM	256 bytes of internal RAM are provided. (0FEC0H~0FFBFH)	external memory area.
A0~A15	High-Impedance state during reset.	Driving state during reset.
P0 (0FFC0H) P1 (0FFC1H) P2 (0FFC4H)	Provided (same chip as TMP90C840A)	R/W function is not provided.
P01CR (0FFC2H)	Provided	EXT, P1C, P0C is not provided.
P2CR (0FFC5H)	Provided	P2XC register is not provided

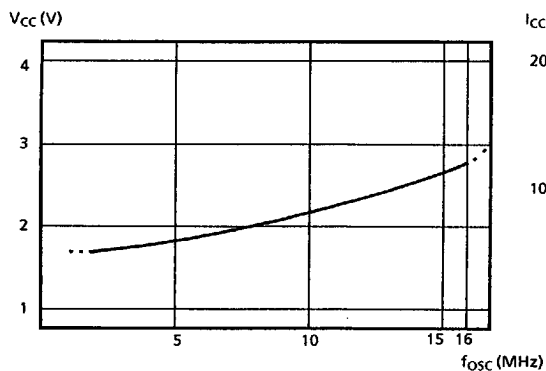
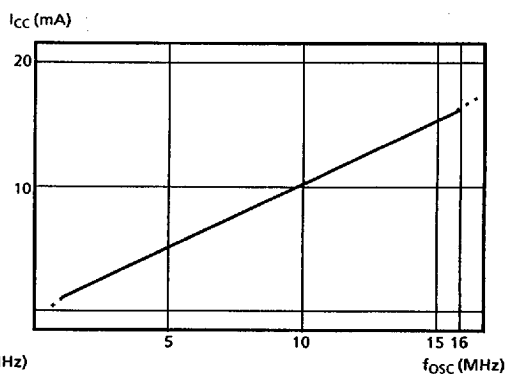
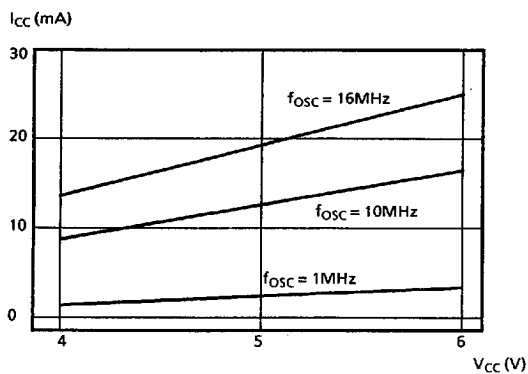
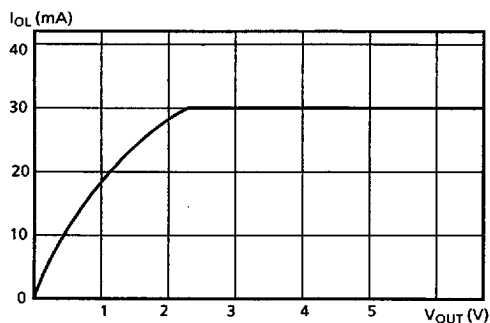
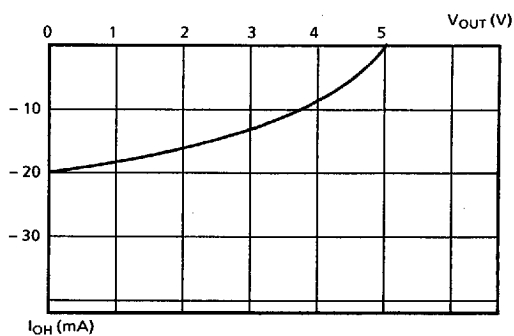
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* Note

Connect $\overline{EA}$ pin with GND pin.

6. TYPICAL CHARACTERISTICS

$V_{CC}=5V$, $T_a=25^\circ C$, unless otherwise noted.

Figure 6 (1) $V_{CC} - f_{OSC}$ TYPICAL CURVEFigure 6 (2) $f_{OSC} - I_{CC}$ TYPICAL CURVEFigure 6 (3) $I_{CC} - V_{CC}$ TYPICAL CURVEFigure 6 (4) $V_{OUT} - I_{OL}$ TYPICAL CURVEFigure 6 (5) $V_{OUT} - I_{OH}$ TYPICAL CURVE

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