Information Storage Devices, Inc.

PRELIMINARY

ISD1012A/1016A/1020A

Single-Chip Voice Record/Playback Devices

FEATURES

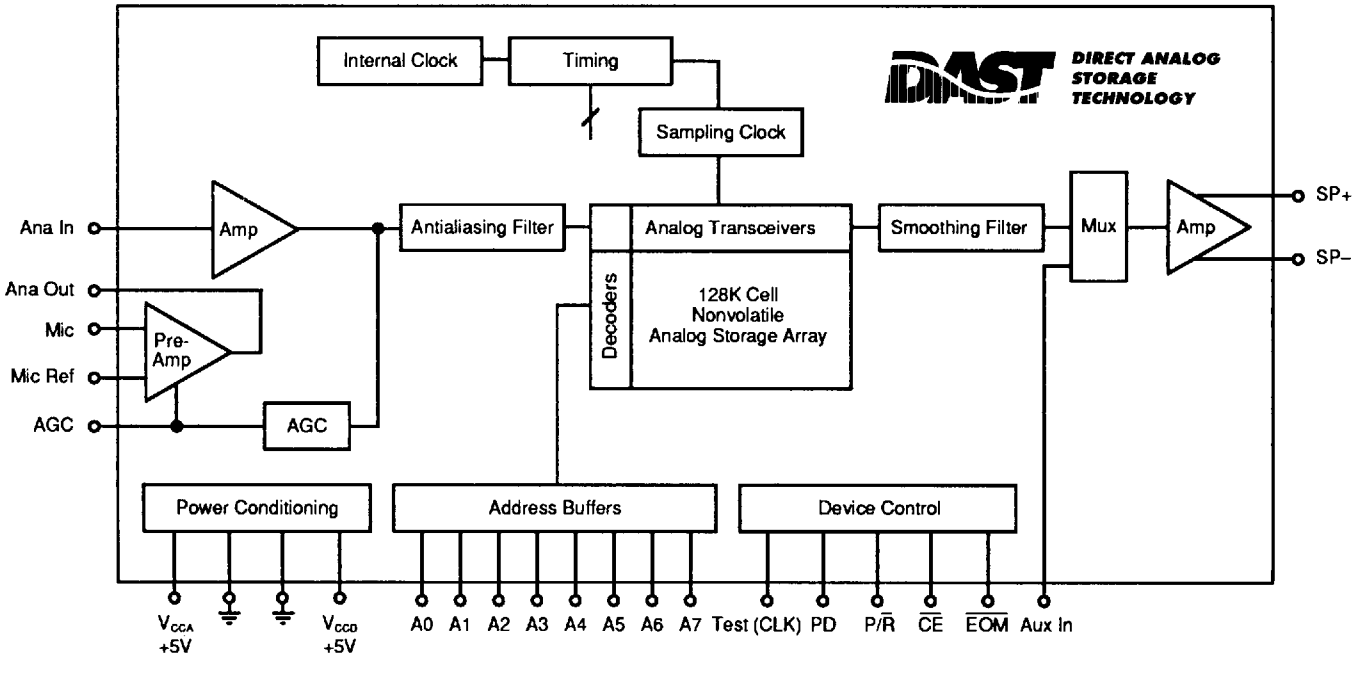
- **Natural, high-quality playback suitable for voice, music, and tones**
- **Single-chip voice record and playback device**
  - Direct analog storage technology
  - Microphone preamplifier
  - Automatic gain control
  - Antialiasing and smoothing filters
  - Speaker amplifier
- **Eliminates digital memory, data converters, modulators, and battery back-up circuits**
- **Easy-to-use; programming and development system not required**
- **Flexible record and playback control options**
- **Nonvolatile EEPROM technology—zero power storage and 10K record cycles**
- **10-year voice retention**
- **Power down mode for lowest power consumption**
- **Single 5-volt power supply**
- **Multiple message address options**
- **Directly cascadable for longer storage duration**
- **Manual switch or microprocessor controllable**
- **Significantly reduced EMI generation and high immunity to external EMI**

ISD1000A FAMILY SUMMARY

The ISD1000A Family includes three device types. ISD1000A Family replaces ISD1000 Family with improved noise characteristics. The ISD1000A Family is fully compatible with the ISD1000 Family. The table summarizes the characteristics of each device.

Part Number	Record/ Playback Duration (seconds)	Input Sample Rate (KHz)	Upper Pass Band Limit (KHz)
ISD1012A	12	10.6	4.5
ISD1016A	16	8	3.4
ISD1020A	20	6.4	2.7

ISD1012A, 1016A, 1020A BLOCK DIAGRAM



GENERAL DESCRIPTION

The ISD1000A Family of devices is designed to record and playback audio and voice information in a single chip with a minimum of circuit complexity. This compact, easy-to-use, nonvolatile, low-power solution has been made possible by ISD's patented DAST™technology—a breakthrough in Direct Analog Storage Technology in EEPROM. ISD's DAST technology results in storage density that is eight times greater than digital memory. The DAST nonvolatile analog array consists of 128K cells—the equivalent of 1M bits of digital storage.

The ISD1000A Family eliminates the need for digital conversion, digital compression, and voice synthesis techniques that often compromise voice quality and complicate usage. The ISD1000A Family of devices includes signal conditioning circuits and control functions which enable a complete, high quality recording and playback system in a single device. The ISD1000A is available in three versions which store voice in 12, 16, or 20 second DAST arrays. Additional devices may be cascaded to achieve longer recording durations. The nonvolatile storage array is based on production-proven, low-power CMOS EEPROM technology.

The highly integrated ISD1000A Family contains all of the basic functions required for high quality voice recording and playback. The noise cancelling Microphone Preamplifier and Automatic Gain Control (AGC) records both low volume and high volume sounds. The AGC attack and release times are adjusted by an external resistor and capacitor. Antialiasing is performed by a continuous fifth-order Chebyshev filter requiring no external components nor clocks to give toll quality reproduction. The low corner of the passband is user-settable by two external capacitors. The devices contain their own temperature-stabilized time-based oscillator.

The ISD1000A devices drive a speaker directly through differential outputs which boosts output by four times and eliminates the need for an output amplifier. A series capacitor requirement is also eliminated. The device will operate from single 5-volt power supplies or from batteries. The device also includes a power down function for applications where minimum power consumption is critical. The CMOS-based design, combined with the nonvolatile storage array, assures lowest possible overall power consumption.

On-chip control functions make the ISD1000A Family very easy to use in virtually any application. Each device offers a variety of operating modes and interface options. The devices may be used in applications that require little more than a few switches and a battery. The devices may also be integrated into electronic systems where digital addresses can be provided for more sophisticated message addressing and control. The ISD1000A DAST arrays are organized in 160 segments. Addresses A0 through A7 provide access to each segment in the array for message addressing. Addressing provides the capability of constructing messages by concatenating stored phrases and sounds.

PIN NAMES

Pin	Pin #	Name
A0–A5	1–6	Address
A6–A7	9, 10	Address
V_{CCD}	28	VCC Digital Power Supply
V_{CCA}	16	VCC Analog Power Supply
V_{SSD}	12	VSS Digital Ground
V_{SSA}	13	VSS Analog Ground
SP+	14	Speaker Output +
SP–	15	Speaker Output –
Test (CLK)	26	Test—Must be tied Low
Aux In	11	Auxiliary Input

Pin	Pin #	Name
Ana Out	21	Analog Output
Ana In	20	Analog Input
AGC	19	Automatic Gain Control
Mic	17	Microphone Input
Mic Ref	18	Microphone Reference
PD	24	Power Down
P/$\overline{R}$	27	Playback/Record
$\overline{EOM}$	25	End-of-Message
$\overline{CE}$	23	Chip Enable

INFORMATION STORAGE DEVICES, INC.

Errata Sheet

ISD1012A/1016A/1020A Data Sheet

February 1992 Revision

Page	Item	Correction
3	DIP and SOIC Pinout	Pin 28 is V_{CCD} not V_{SSD}. Pin 26 is Test (CLK). Mic pin is Pin 17.
	PLCC Pinout	Package dot should be below Pin 1.
4	Power Down (PD)	Insert "Low" in last sentence. Sentence should read "When $\overline{EOM}$ goes Low for overflow . . ."
	Chip Enable ($\overline{CE}$)	Last sentence should read "If the ISD1000A is not selected and is in the playback mode, then when $\overline{CE}$ is taken High, the auxiliary input is directed to the speaker amplifier."
	Address Inputs (A0–A7)	Table should read ISD1020A not ISD10120A.
5	Table 1. Operational Modes	All references to EOM and CE should have a bar over the reference.
6	Design Schematic	Capacitor between pins 20 and 21 should be C3 not C1.
7	DC Parameters	$Typ_{(0)}$ should read $Typ_{(1)}$.

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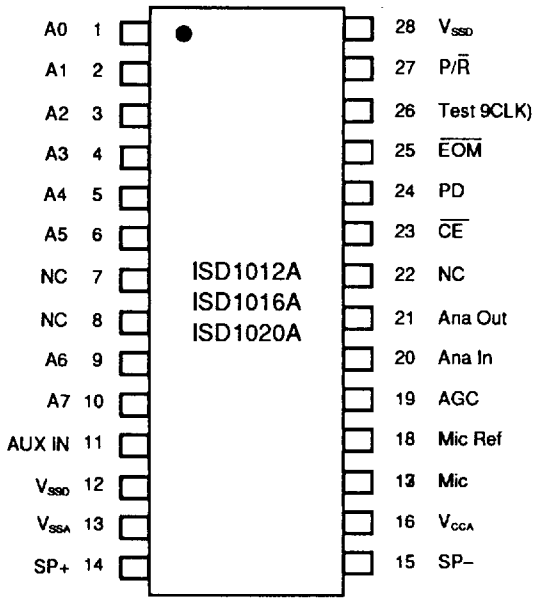
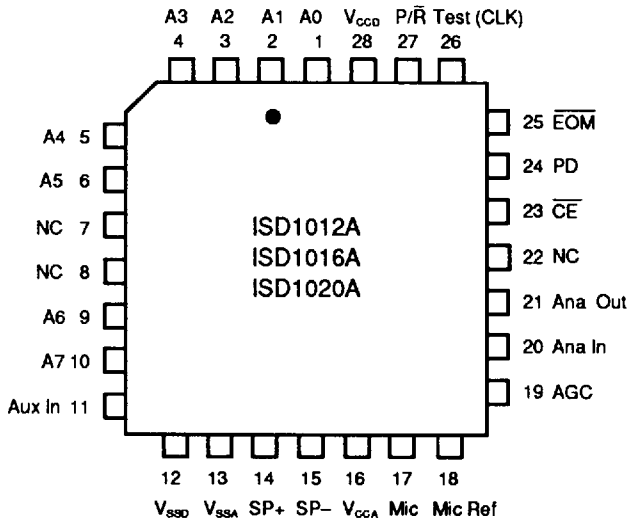
ISD1000A FAMILY PIN ASSIGNMENTS



DIP and SOIC



PLCC

ISD1000A FAMILY PIN DESCRIPTIONS

Microphone Input (Mic)

The microphone is AC-coupled to this pin via a series capacitor. The user-selectable value of the input series capacitor (together with the 10K ohm resistance internal to the ISD1000A) determines the low frequency cut-off for the ISD1000A passband.

Microphone Reference (Mic Ref)

When AC is coupled to microphone ground, the recorded noise level is significantly reduced. Ground noise is referenced to the preamplifier. If this pin is not used, it must NOT be connected to any signal or voltage. It must float.

Analog Output (Ana Out)

The microphone signal is amplified and is output to the Ana Out pin. The voltage gain of the pre-amp is determined by the voltage level at the Automatic Gain Control (AGC) pin. It has a maximum gain of about 24dB for small input signal levels.

Analog In (Ana In)

The external capacitor connects Ana In to the Ana Out pin. The value of the external capacitor, together with the 2.7KΩinput impedance at Ana In, can be chosen to give additional cut-off at the low frequency end of the voice passband. The Ana In pin may also be used to input alternative sources of analog signal, other than the microphone signal.

Automatic Gain Control (AGC)

The purpose of the AGC is to dynamically adjust the preamplifier gain, and therefore extend the range of input signals which can be applied to the microphone input without distortion. The AGC considerably extends the range of recordable sounds from whispers to loud voices. Peak voltage levels at the Amplifier output are detected in the AGC circuit, and charge the external capacitor C2 on the AGC Control pin. The source resistance (5K) of the internal AGC circuit and the external capacitor C2 determine the "attack" time of the gain control. "Release" time is determined by the RC time constant of the external resistor (R2) and capacitor (C2). For AGC voltages of 1.5V and below, the preamplifier is at its maximum gain 24dB. Reduction in preamplifier gain occurs for voltages of approximately 1.8V.

Speaker Outputs (SP+/SP-)

The SP+ and SP- pins provide direct drive for loudspeakers with impedances as low as 16 ohms. A single output may be used, but, for direct drive loudspeakers, the two opposite polarity outputs give an improvement in output power of up to four times over a single-ended connection. Furthermore, when SP+ and SP- connections are used, a speaker coupling capacitor is not required. A single-ended connection will require an AC coupling capacitor between the SP pin and the speaker. The speaker outputs are held at V_{SSA} during recording and Power Down.

PIN DESCRIPTION, *continued*

Power Down (PD)

The Power Down pin is taken high (when not recording or playing back) to provide a very low power mode to the ISD1000A. When $\overline{EOM}$ goes for overflow condition, PD must be brought High to reset addresses.

Chip Enable($\overline{CE}$)

The Chip Enable pin is taken low to enable all playback and record operations. The address inputs (A0-A7) and the playback/record input are latched into the ISD1000A by this falling edge. When $\overline{CE}$ is taken high, the ISD1000A is unselected, and the auxiliary input is directed into the speaker power amplifier.

Playback/Record (P/$\overline{R}$)

The state of the P/$\overline{R}$ is latched into the ISD1000A on the falling edge of $\overline{CE}$. A High level selects a playback cycle, while a Low level selects a record cycle. During record, the playback circuits and speaker output amplifiers are powered down, and the SP+ and SP– outputs are held at V_{SSA}. During playback, the internal record and analog inputs are disabled. In playback mode, it is only necessary to supply the starting message address. The ISD1000A will playback until an End-of-Message is encountered (see Table 1, Page 5 for other options). In record mode, the start address determines the beginning of the message. The ISD1000A Family records until $\overline{CE}$ is brought High or until an overflow is detected.

Address Inputs (A0-A7)

The Address Inputs provide two functions in the ISD1000A Family:

(1) Message address (A6 OR A7 = Low)

(2) ISD1000A Family Operational Mode Options (A6 AND A7 = High)

Operational mode options are shown in Table 1 (Page 5). There are a maximum of 160 message addresses (or segments). Each segment corresponds to one of 160 rows in the analog storage array. The message addresses (segments) are in locations 0 through 159 contiguous. The playback/record duration of each segment depends on the device and is as follows:

Family Member	Segment Playback/Record Duration (seconds)
ISD1012A	0.075
ISD1016A	0.100
ISD10120A	0.125

An operation may be started at any address, as defined by address pins A0-A7. Record or playback continues with automatic incrementing of internal on-chip address until either $\overline{CE}$ is brought high (record), an end of message bit is encountered (playback with $\overline{CE}$ high) or an overflow (device full) condition results.

Test (CLK)

Test (CLK) is normally only used by manufacturing for test. In applications circuits it is tied to ground, however, if greater timing precision is desired, (internal clock has ± 2% tolerance over temperature and voltage range) the chip can be externally clocked through this pin.

For the ISD1016A this clock is a 1024 KHz signal; the ISD1012A is 1365 KHz; and the ISD1020A is 819 KHz. The duty cycle is not critical, as this clock is immediately divided by two.

End of Message ($\overline{EOM}$)

A digital End-of-Message marker is automatically inserted in an internal nonvolatile register at the end of each recorded message. The $\overline{EOM}$ output goes Low under the following conditions:

- At end of each message
- Message overflow (device full)

The ISD1000A Family has an internal V_{CC} detect circuit. When V_{CCD} drops below 3.5V, $\overline{EOM}$ is forced Low and the device is placed in playback mode. The $\overline{EOM}$ marker provides a convenient handshake signal for a processor. The $\overline{EOM}$ function also facilitates cascading.

Auxiliary Input (Aux-In)

The input to the internal output power amplifier is multiplexed between the storage array and the auxiliary input pin. The auxiliary input is active when $\overline{CE}$=High and playback has ended or $\overline{EOM}$=Low due to overflow. The active power amplifier input (storage array or auxiliary input) inhibits the other input. (For noise considerations, it is suggested that the auxiliary input not be driven when the storage array is active.) The Auxiliary Input also facilitates cascading.

V_{CCA} and V_{CCD} (+5.0 Volts)

Analog and digital circuits internal to the ISD1000A Family use separate power buses to minimize noise on the chip. These +5 Volt buses are brought out to separate pins on the package and should be tied together as close to the supply as possible. It is important that the +5 Volt supply be decoupled as close as possible to the package.

V_{SSA} and V_{SSD} (Ground)

Similar to V_{CCA} and V_{CCD} the analog and digital circuits internal to the ISD1000A Family use separate ground buses to minimize noise. These pins should be tied together as close as possible to the device.

OPERATIONAL MODES

The ISD1000A Family can be used in systems with various levels of control sophistication, from microprocessor-controlled environments to simple push-buttons or switches. Different operational modes are enabled by taking address pins A7 AND A6 HIGH. In this mode, the states of address pins A5 through A0 determine the control function and NOT the message address. The options are shown in the Table below. Each option is selected by bringing the appropriate address High. Multiple options may be selected by applying a High level to each of the desired address pins.

Table 1. Operational Modes

Function	Address Control (High)	Pin #	Typical Use
Message cueing (speaker output disabled). (See Note 1)	A0	1	Selecting messages when address is unknown. Indirect message addressing.
EOM markers are deleted by the next message use with (A4 = 1). (Available Q3/1992)	A1	2	Position a single EOM marker at the end of the last message.
During playback, EOM pulses low at array overflow only (used for cascading function).	A2	3	Playing back messages whose duration exceeds a single chip limitation.
Continuous playback (at EOM loops back to beginning and repeats message).	A3	4	Continous repeat.
Consecutive addressing – Message start pointer is reset only when operational mode is changed (playback/record). (See Note 2)	A4	5	Recording consecutive multiple messages.
Playback is chip enable level activated.	A5	6	Terminate playback with CE.

Notes:

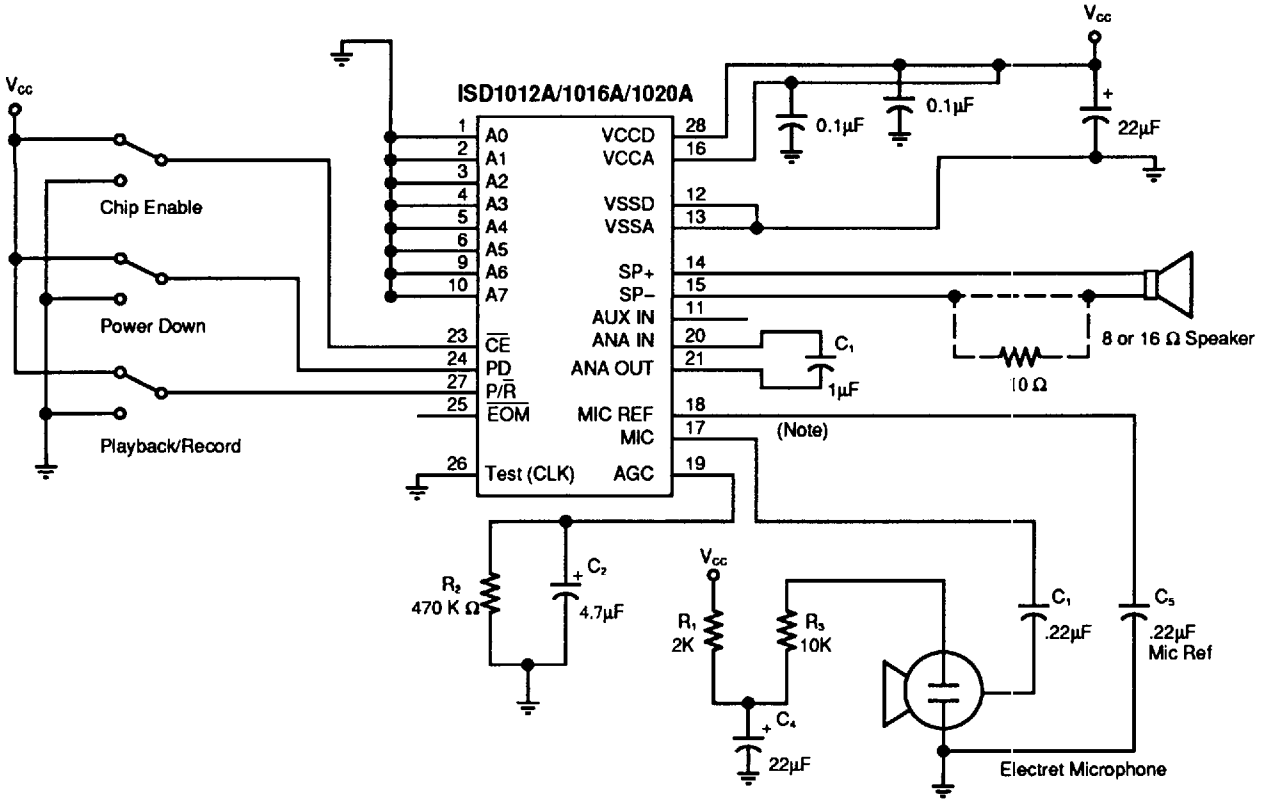
1. Message Cueing (Available Q3, 1992)

Message cueing allows the user to skip through messages. Each time $\overline{CE}$ memory is pulsed Low with the address inputs set to this mode, the internal message pointer skips forward until it encounters an end-of-message marker and then stops. By providing a certain number of pulses to the $\overline{CE}$ pin in message cueing mode and then changing to consecutive addressing mode, the user can select and then record or playback a desired message. Message cueing should not be used in Record mode.

2. Consecutive Addressing

Consecutive addressing allows for recording and playback of consecutive messages without the need for direct addressing or any other kind of message management. During recording, each time that $\overline{CE}$ is taken Low, a message is recorded at the next position in memory. When $\overline{CE}$ is taken High again, an End-of-Message marker is written to indicate the position of the End of the message. In this fashion, a string of messages is recorded, each one placed immediately after the previous one.

APPLICATION EXAMPLE— DESIGN SCHEMATIC



Note: If desired, this pin may be left unconnected (microphone preamplifier noise will be higher). In this case, pin 18 must not be tied to any other signal or voltage.

APPLICATION EXAMPLE— BASIC DEVICE CONTROL

Control Step	Function	Action
1	Power-up chip and select record/playback mode	1. PD = Low 2. P/$\overline{R}$ = As desired
2	Set message address for record/playback	Set addresses A0–A7
3	Begin record/playback	$\overline{CE}$ = Low
4	End cycle	$\overline{CE}$ = High

APPLICATION EXAMPLE-- PASSIVE COMPONENT FUNCTIONS

Part	Function	Comments
R1	Microphone power supply decoupling network	Reduces power supply noise
R2	Release time constant	Sets release time for AGC
R3	Microphone biasing resistor	Provides biasing for microphone operation
C1	Microphone DC-blocking capacitor. Low frequency cutoff	Decouples microphone bias from chip. Provides single-pole low frequency cutoff
C2	Attack/Release time constant	Sets attack/release time for AGC
C3	Low frequency cutoff capacitor	Provides additional pole for low frequency cutoff
C4	Microphone power supply decoupling network	Reduces power supply noise
C5	Noise reduction	Reduces input noise

ABSOLUTE MAXIMUM RATINGS (ISD1012A/1016A/1020A)

Condition	Value
Operating Temperature	0° C to +70° C
Temperature under bias*	–65° C to +125° C
Storage temperature range*	–65° C to +150° C
Voltage applied to any pin*	(V_{SS} –0.3 V) to (V_{CC} + 0.3 V)
Voltage applied to any pin (input current limited to ± 20 mA)*	(V_{SS} –1.0 V) to (V_{CC} + 1.0 V)
Lead temperature (soldering –10 seconds)*	300° C
$V_{CC} - V_{SS}$	-0.3 V to +7.0 V

* Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings denoted by (*) may affect device reliability. Stress ratings denoted by (*) do not imply functional operation at these conditions.

DC PARAMETERS (ISD1012A/1016A/1020A)

Operating Conditions T_A = 0° C to 70° C (Note #4); V_{CC} (Note #5) = 5.0 V ± 10%; V_{SS} (Note #6) = 0 V; Unless otherwise noted

Symbol	Parameters	Min	Typ(0)	Max	Units	Conditions
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –1.6 mA
V_{OH1}	Output High Voltage	V_{CC} –0.4			V	I_{OH} = –10 µA
I_{CC}(7)	V_{CC} Current (Operating)			25	mA	R_{EXT} = ∞
I_{SB}(7)	V_{CC} Current (Standby)		1	10	µA	
I_{IL}	Input Leakage Current			±1	µA	
R_{EXT}	Output Load Impedance	16			Ω	Speaker Load
R_{MIC}	Pre-Amp In Input Resistance Pins 17 and 18		10		KΩ	
R_{AUX}	Aux Input Resistance		10		KΩ	
R_{ANA} In	Ana In Input Resistance		2.7		KΩ	
A_{PRE1}	Pre-Amp Gain 1		24		dB	AGC = 0.0 V
A_{PRE2}	Pre-Amp Gain 2			5	dB	AGC = 2.5 V
A_{AUX}	Aux In/SP + Gain	0.9		1.0	V/V	
A_{ARP}	Ana In to SP+/–		22		dB	
R_{AGC}	AGC Output Resistance		5		KΩ	
I_{PREH}	Pre-Amp Out Source		100		µA	@V_{OUT} = 1.0 V
I_{PREL}	Pre-amp In Sink		100		µA	@V_{OUT} = 2.0 V

ISD1012A—12-SECOND DURATION DEVICE AC PARAMETERS

Operating Conditions T_A = 0° C to 70° C (Note #4); V_{CC} (Note #5) = 5.0 V ± 10%; V_{SS} (Note #6) = 0 V; Unless otherwise noted

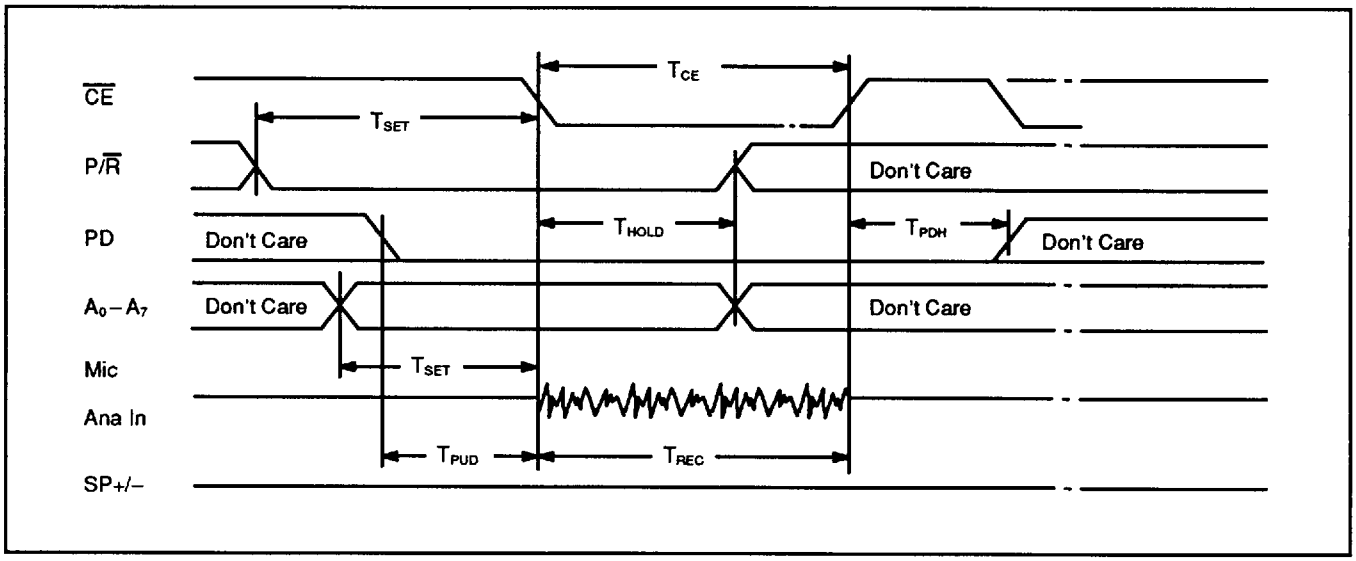
Symbol	Characteristics	Min	Typ(0)	Max	Units	Conditions
FS	Internal Clock Sampling Frequency		10.6		KHz	
BW	Passband (3)		4500		Hz	
THD	Total Harmonic Distortion		2		%	@ 1KHz
P_{OUT}	Speaker Output Power			50	mW	R_{EXT} = 16Ω
V_{OUT}	Voltage across speaker pins			2.5	Vp-p	R_{EXT} = 600Ω
V_{IN1}	Mic input voltage			20	mv	Peak - Peak (2)
V_{IN2}	Ana In input voltage			50	mv	Peak - Peak
V_{IN3}	Aux In input voltage			1.25	V	Peak - Peak; R_{EXT} = 16Ω
T_{SET}	Control/Address set-up	300			nsec	
T_{HOLD}	Control/Address hold	0			nsec	
T_{CE}	$\overline{CE}$ Record time	100			nsec	
T_{PUD}	Power up delay	18.75			msec	
T_{PDH}	Power down hold	0			nsec	
T_{REC}	Record time		12		sec	
T_{PLAY}	Playback time		12		sec	
T_{EOM}	$\overline{EOM}$ pulse width		9.4		msec	

Notes:

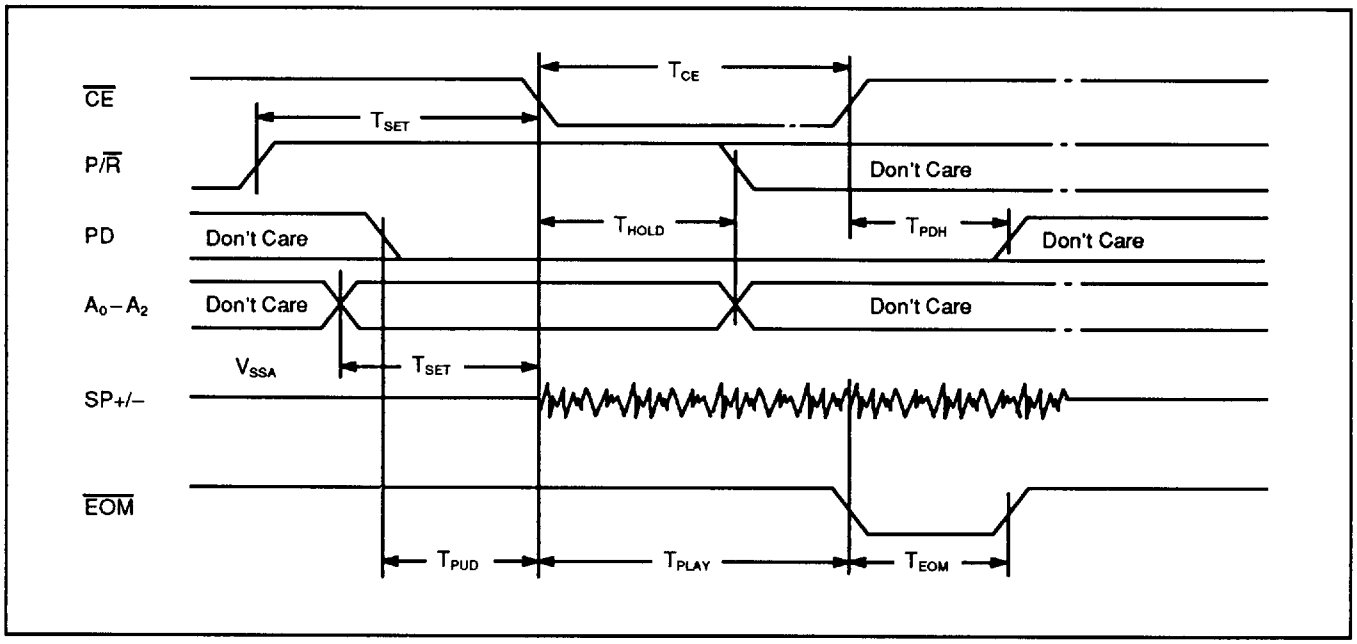
1. Typical values @ T_A = 25° C and nominal voltages
2. With 12 KΩ series resistor at Ana In
3. Low frequency cutoff depends on value of external capacitors (see Pin Descriptions).
4. Case temperature
5. $V_{CC} = V_{CCD} = V_{CCA}$
6. $V_{SS} = V_{SSA} = V_{SSD}$
7. V_{CCA} and V_{CCD} connected together

TIMING DIAGRAMS (ISD1012A)

RECORD



PLAYBACK



ISD1016A—16-SECOND DURATION DEVICE AC PARAMETERS

Operating Conditions T_A = 0° C to 70° C (Note #4); V_{CC} (Note #5) = 5.0 V ± 10%; V_{SS} (Note #6) = 0 V; Unless otherwise noted

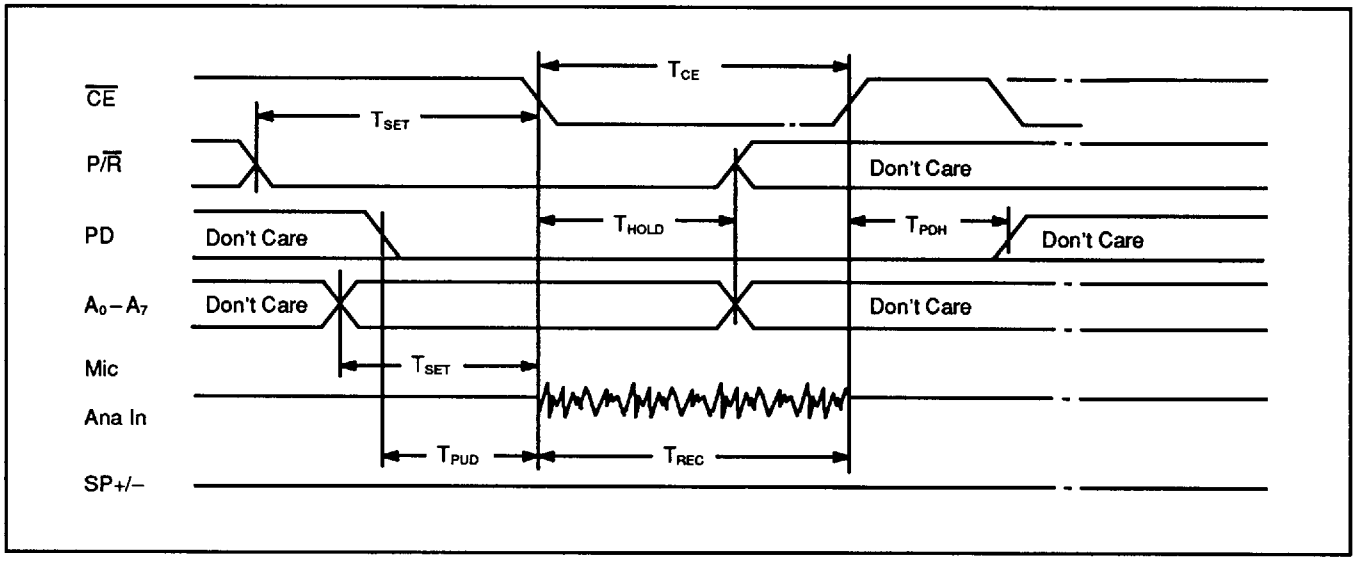
Symbol	Characteristics	Min	Typ(◊)	Max	Units	Conditions
FS	Internal Clock Sampling Frequency		8		KHz	
BW	Passband (3)		3400		Hz	
THD	Total Harmonic Distortion		2		%	@ 1KHz
P_{OUT}	Speaker Output Power			50	mW	R_{EXT} = 16Ω
V_{OUT}	Voltage across speaker pins			2.5	Vp-p	R_{EXT} = 600Ω
V_{IN1}	Mic input voltage			20	mv	Peak – Peak (2)
V_{IN2}	Ana In input voltage			50	mv	Peak – Peak
V_{IN3}	Aux In input voltage			1.25	V	Peak – Peak; R_{EXT} = 16Ω
T_{SET}	Control/Address set-up	300			nsec	
T_{HOLD}	Control/Address hold	0			nsec	
T_{CE}	$\overline{CE}$ Record time	100			nsec	
T_{PUD}	Power up delay	25			msec	
T_{PDH}	Power down hold	0			nsec	
T_{REC}	Record time		16		sec	
T_{PLAY}	Playback time		16		sec	
T_{EOM}	$\overline{EOM}$ pulse width		12.5		msec	

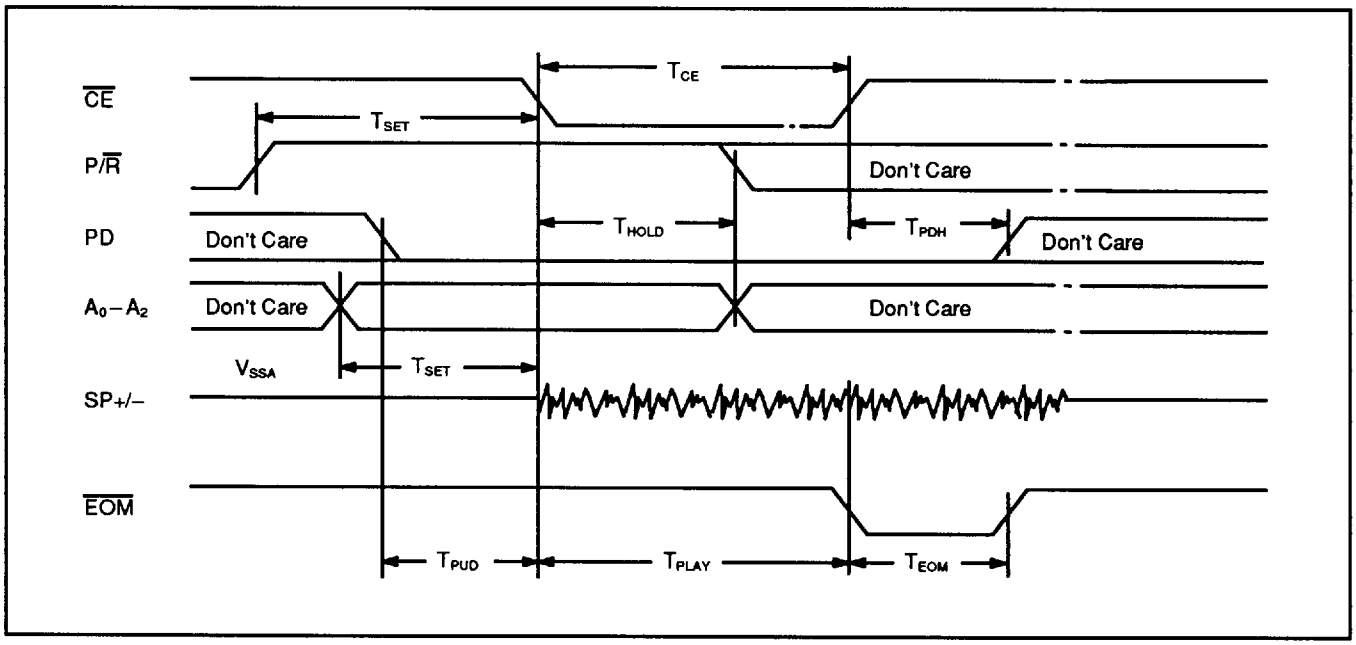
Notes:

1. Typical values @ T_A = 25° C and nominal voltages
2. With 12 KΩ series resistor at Ana In
3. Low frequency cutoff depends on value of external capacitors (see Pin Descriptions).
4. Case temperature
5. $V_{CC} = V_{CCD} = V_{CCA}$
6. $V_{SS} = V_{SSA} = V_{SSD}$
7. V_{CCA} and V_{CCD} connected together

TIMING DIAGRAMS (ISD1016A)

RECORD





ISD1020A—20-SECOND DURATION DEVICE AC PARAMETERS

Operating Conditions T_A = 0° C to 70° C (Note #4); V_{CC} (Note #5) = 5.0 V ± 10%; V_{SS} (Note #6) = 0 V; Unless otherwise noted

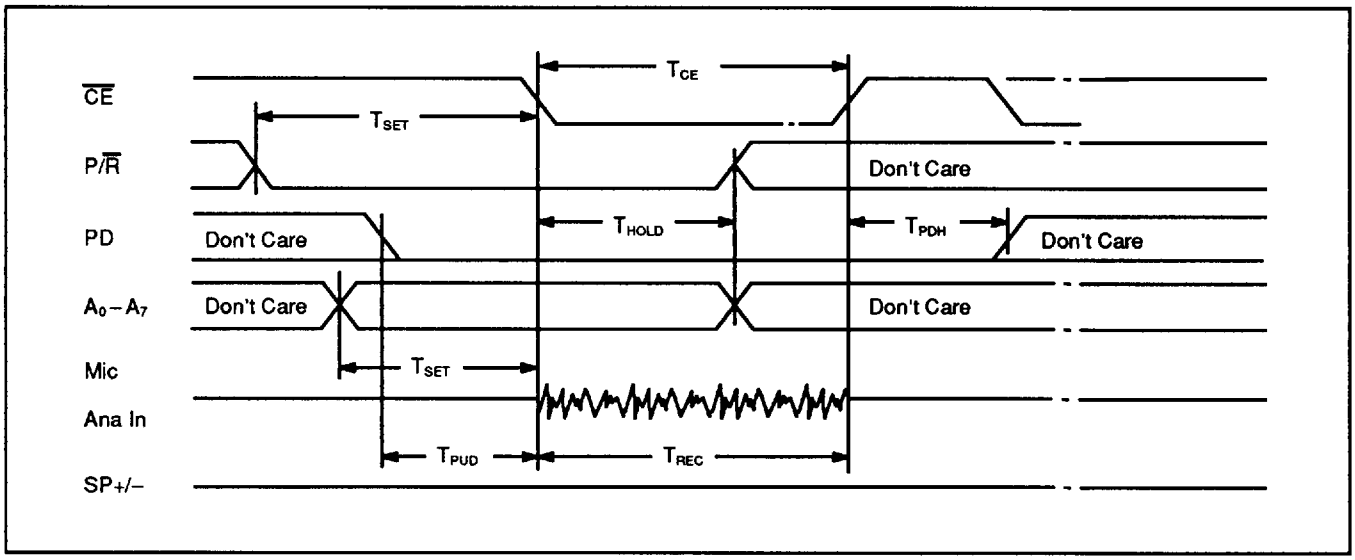
Symbol	Characteristics	Min	Typ(1)	Max	Units	Conditions
FS	Internal Clock Sampling Frequency		6.4		KHz	
BW	Passband (3)		2700		Hz	
THD	Total Harmonic Distortion		2		%	@ 1KHz
P_{OUT}	Speaker Output Power			50	mW	R_{EXT} = 16Ω
V_{OUT}	Voltage across speaker pins			2.5	Vp-p	R_{EXT} = 600Ω
V_{IN1}	Mic input voltage			20	mv	Peak – Peak (2)
V_{IN2}	Ana In input voltage			50	mv	Peak – Peak
V_{IN3}	Aux In input voltage			1.25	V	Peak – Peak; R_{EXT} = 16Ω
T_{SET}	Control/Address set-up	300			nsec	
T_{HOLD}	Control/Address hold	0			nsec	
T_{CE}	$\overline{CE}$ Record time	100			nsec	
T_{PUD}	Power up delay	31.25			msec	
T_{PDH}	Power down hold	0			nsec	
T_{REC}	Record time		20		sec	
T_{PLAY}	Playback time		20		sec	
T_{EOM}	$\overline{EOM}$ pulse width		15.6		msec	

Notes:

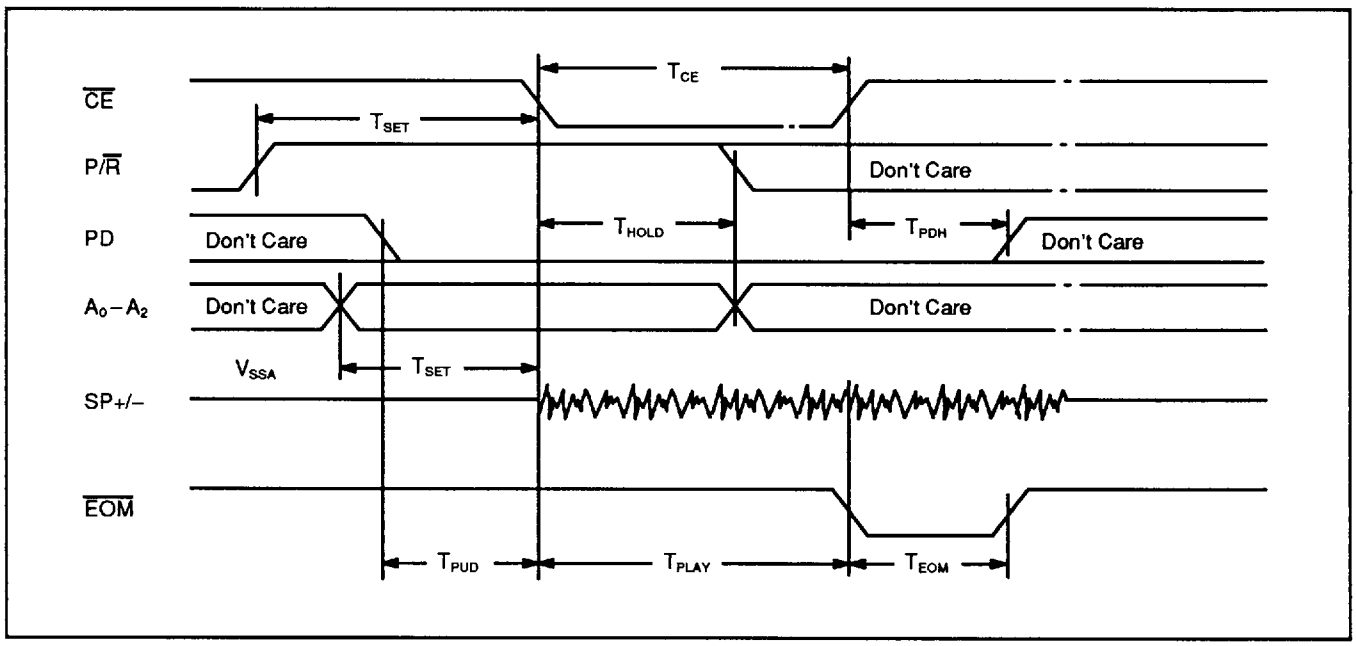
1. Typical values @ T_A = 25° C and nominal voltages
2. With 12 KΩ series resistor at Ana In
3. Low frequency cutoff depends on value of external capacitors (see Pin Descriptions).
4. Case temperature
5. $V_{CC} = V_{CCD} = V_{CCA}$
6. $V_{SS} = V_{SSA} = V_{SSD}$
7. V_{CCA} and V_{CCD} connected together

TIMING DIAGRAMS (ISD1020A)

RECORD

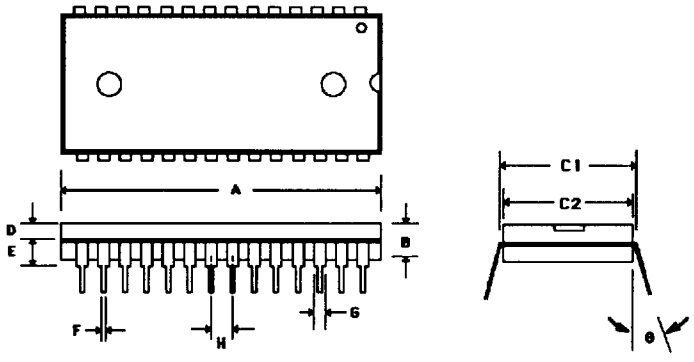


PLAYBACK



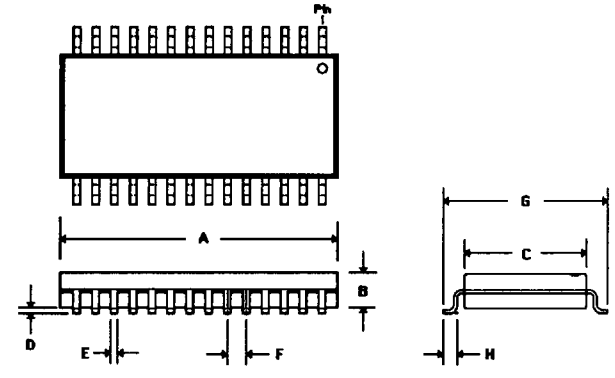
PACKAGE DIAGRAMS

28-lead Plastic Dual In-line Package (DIP) Type P



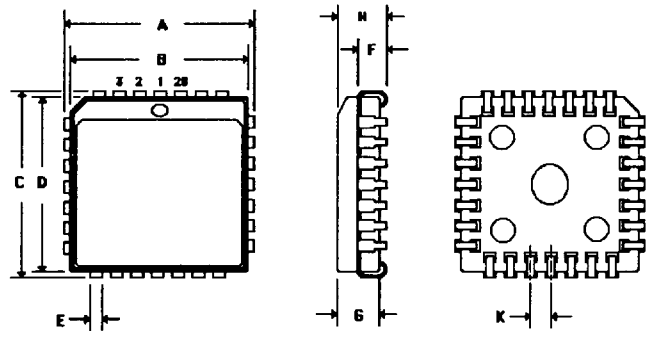
	INCHES			MILLIMETERS		
	MIN	NOM	MAX.	MIN	NOM	MAX.
A	1.445	1.450	1.455	36.7	36.83	36.95
B		.150			3.89	
C1	.600		.625	15.24		15.88
C2	.530	.540	.550	13.46	13.72	13.97
D	1.25	1.30	1.35	2.92	3.05	3.18
E	.125	.130	.135	3.18		3.43
F	.015	.018	.022	0.38	0.46	0.56
G	.055	.060	.065	1.40	1.52	1.65
H		.100			2.54	
θ	0°	7°	15°	0°	7°	15°

28-lead Plastic Small Outline Package (SOIC) Type G



	INCHES			MILLIMETERS		
	MIN	NOM	MAX.	MIN	NOM	MAX.
A	.706	.714	.718	17.93	18.14	18.24
B	.086	.088	.090	2.18	2.24	2.29
C	.340	.346	.350	8.64	8.79	8.89
D	.004	.007	.010	.102	.178	.254
E	.014	.016	.020	.360	.410	.480
F		.050			1.27	
G	.463	.470	.477	11.76	12.00	12.12
H	.020	.031	.042	.510	.790	1.07

28-lead Plastic Leadless Chip Carrier (PLCC) Type J



	INCHES			MILLIMETERS		
	MIN	NOM	MAX.	MIN	NOM	MAX.
A	.485	.490	.495	12.32	12.45	12.57
B	.450	.452	.454	11.43	11.48	11.53
C	.485	.490	.495	12.32	12.45	12.57
D	.450	.452	.454	11.43	11.48	11.53
E	.026		.032			
F	.100	.101	.110	2.54	2.56	2.79
G	.148	.152	.156	3.76	3.86	3.96
H	.165	.172	.180	4.19	4.37	4.57
K		.050				

Unless otherwise specified:
all tolerances are ± .007 inches

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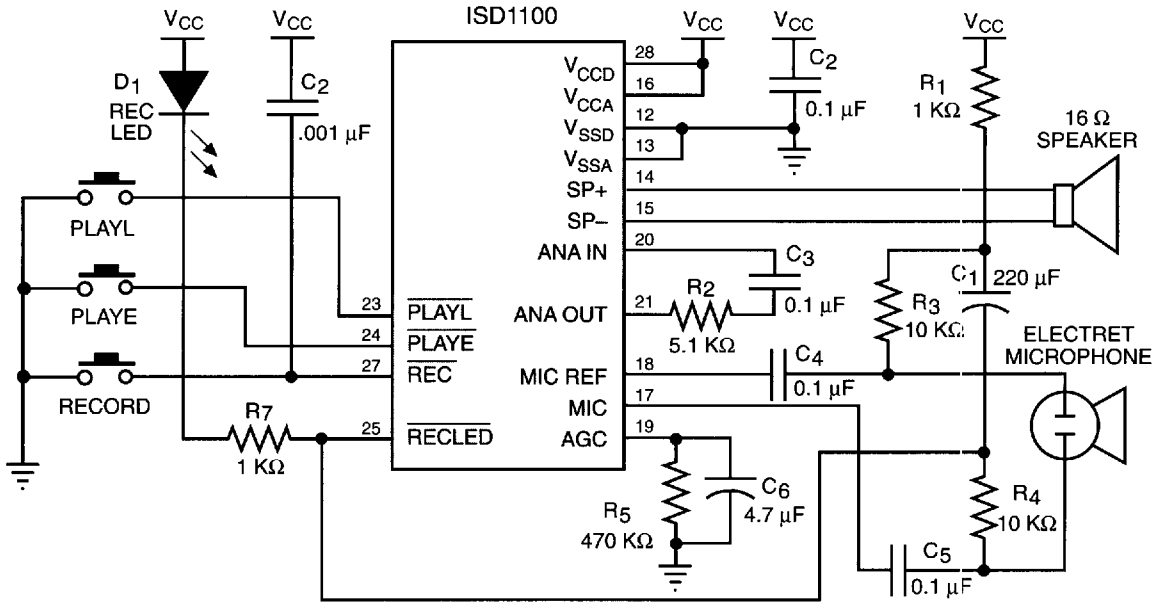
Information contained in this ISD1000A Family product specification supersedes all data for the ISD1000A Family products published by ISD before February, 1992.

ORDERING INFORMATION

When placing an order for the ISD1000A Family of devices, please refer to the following model numbers:

Model Number	Record/Playback Duration (Seconds)	Description
ISD1012AP	12	28-pin plastic dual in-line package
ISD1012AJ	12	28-lead plastic leadless chip carrier (PLCC)
ISD1012AG	12	28-lead small outline integrated circuit (SOIC)
ISD1012AX	12	Bare unpackaged die
ISD1016AP	16	28-pin plastic dual in-line package
ISD1016AJ	16	28-lead plastic leadless chip carrier (PLCC)
ISD1016AG	16	28-lead small outline integrated circuit (SOIC)
ISD1016AX	16	Bare unpackaged die
ISD1020AP	20	28-pin plastic dual in-line package
ISD1020AJ	20	28-lead plastic leadless chip carrier (PLCC)
ISD1020AG	20	28-lead small outline integrated circuit (SOIC)
ISD1020AX	20	Bare unpackaged die

APPLICATION SCHEMATIC



Additional components may be required for some applications.
For more details, please refer to the ***ISD Application Notes and Design Manual.***

FUNCTIONAL DESCRIPTION EXAMPLE

The following example operating sequence demonstrates the functionality of the ISD1100 Series devices.

1. Record a message filling the memory.

Pulling the $\overline{\text{REC}}$ signal LOW initiates a record cycle from the beginning of the message space. If $\overline{\text{REC}}$ is held LOW, the recording continues until the message space has been filled. Once the message space is filled, recording ceases. The device will automatically power down after $\overline{\text{REC}}$ is released HIGH.

2. Edge-activated playback.

Pulling the $\overline{\text{PLAYE}}$ signal LOW initiates a playback cycle from the beginning of the message space. The rising edge of $\overline{\text{PLAYE}}$ has no effect on operation. If a recording has filled the message space, the entire message is played. When the device reaches the end of the message space, it automatically powers down. A subsequent falling edge on $\overline{\text{PLAYE}}$ initiates a new play cycle from the beginning of the memory.

3. Level-activated playback.

Pulling the $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle from the beginning of the message space. If $\overline{\text{PLAYL}}$ remains LOW, the device plays through to the end of the message and subsequently enters the power-down mode.

4. Level-activated playback (truncated).

If $\overline{\text{PLAYL}}$ is pulled HIGH any time during the playback cycle, the device stops playing and enters the power-down mode.

5. Record (interrupting playback).

The $\overline{\text{REC}}$ signal takes precedence over other operations. Any LOW-going transition on $\overline{\text{REC}}$ initiates a new record operation from the beginning of the memory, regardless of any current operation in progress.

6. Record a message, partially filling the memory.

A record operation need not fill the entire memory. Releasing the $\overline{\text{REC}}$ signal HIGH before filling the message space causes the recording to stop and an end-of-message marker to be placed. The device powers down automatically.

7. Play back a message, partially filling the memory.

Pulling the $\overline{\text{PLAYE}}$ or $\overline{\text{PLAYL}}$ signal LOW initiates a playback cycle which is then completed when the end-of-message marker is encountered. Playback ceases and the device powers down.

8. $\overline{\text{RECLED}}$ operation.

The $\overline{\text{RECLED}}$ output pin provides an active-LOW signal which can be used to drive an LED as a "record in progress" indicator. It returns to a HIGH state when the $\overline{\text{REC}}$ pin is released HIGH or when the recording is completed due to the memory being filled.